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| Revision | Date | Description | Author |
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|  |  |  |  |
| 0.5 | 2021/Dec. | Proposed version | Anindita RC |
| 0.1 | 2021/Nov. | Draft version | Anindita RC |

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| Where guides exists they may be found on the BCaM process website on the ‘Templates’ page where BCaM templates can be downloaded. The guide is indicated by an icon:.  Fields are shown by shaded text. Do not replace these fields by typing them over in the text itself. Either enter the correct value for these fields using File/Properties/Custom (enter the Value field and click ‘Modify’) or at File/Properties/Summary and/or let some of these fields automatically be filled in by using the IMPULSE-BCP / MS Office interface, after checking the document in IMPULSE-BCP (only if used). Further guidance can be found in the FAQs on the NXP BCaM Process website under General Info.  Text between angle brackets and that are not fields (so no shaded text), like <YYYYMMDD>, should be updated by replacing them with the correct text.  Before publication, please delete all ‘information text’ tables. Highlight the empty paragraph preceding the table, highlight the table (including the end of row markers) and select ‘Cut’ from the ‘Edit’ menu.  Revision History of the template   |  |  |  |  | | --- | --- | --- | --- | | Revision | Date | Description | Author | | 1.0 | 20110916 | First release based on BCaM\_SAM\_lt\_02\_sttmnt-of-work.doc | Automotive Project Office | |  |  |  |  | |

Revision History

Contents

# Document purpose

## Purpose

The purpose of this document is to provide a Detailed Technical Specification (DTS) of the RFE Analog Test Bus (ATB) IP design for project *Smart TRX* (STRX).

RFE Analog Test Bus (ATB) IP is a sub-module within the RFE system of STRX SoC. ATB provides infrastructure to monitor the important signals ( current / voltage ) of internal analog IPs and also to force appropriate test signals to these IPs for characterizing their performance.

## Scope

The scope is to cover the implementation details of the ATB IP.

## Target audience

Target audience is:

* architects (Front End integration)
* IP owners (analog/AMS interfacing)
* digital (interface)
* DfT
* software
* Verification, Validation, and Test Work-Packages
* Back End integration

# Introduction

RFE ATB IP is the central connection block between the RFE system and external validation/test environment. It also enables various IP trimming and FuSa sensing of critical internal nodes. ATB Functional diagram

|  |
| --- |
| Shape  Description automatically generated with medium confidence  Test + val ValValida  Test+val+FuSa |

Figure 1 Simplified block diagram of RFE ATB IP

## Features

Broadly speaking, ATB provides the infrastructure to test other RFE IPs falling in the following three categories-

1. **DC ATB** : Bidirectional, differential bus for testing IPs by sensing / forcing DC signals ( currents/voltages ). There are two DC ATB units within RFE ATB , each incorporates a 10-bit SAR ADC for digitizing signals. This is part of FuSa mechanism.
2. **AC ATB** : Bidirectional, differential bus for testing IPs by sensing / forcing AC signals ( <40MHz , eg. RX , RX-ADC ). Includes an AC buffer to drive external load.
3. **RF Buffer** : For buffering GHz signals ( 5GHz ChirpPLL , 2.56GHz ClockPLL ) to external equipment ( 50 ohms) for phase noise measurement. It has Single ended output and programmable output power.

# Pin description

## ida\_mmw\_rfe\_atb\_top

Table 1. Pin description top-level ida\_mmw\_rfe\_atb\_top

|  |  |  |
| --- | --- | --- |
| **Signal name**  **& index** | **Signal type[[1]](#footnote-1)** | **Description (short)** |
| **Supplies/Grounds** | |  |
| vdda\_ 1v8 | P | analog supply; 1.8V±5% (supplies ATB sub-module, part of Functional Safety feature) |
| vdda\_1v45 | P | analog supply; 1.45V±5% |
| vddd | P | digital supply; 0.9V±5% |
| vssa\_1v8 | G | analog ground; return path for *vdda\_1v8* |
| vssa | G | analog ground; return path for *vdda\_1v45* |
| vssd | G | digital ground; return path for *vddd* |
| **Interface IO signals (digital)** | |  |
| bg\_ok\_flag | DO | digital flag to indicate the bandgap circuit (BG0V9) has started up. Only available after signal *pon\_ls* is ‘H’.  Active high |
| pon\_ls\_atb | I | PowerON LevelShifter(s); signal releases the levelshifters for digital (Vddd) domain to analog domain conversion. |
| **LLDO signals** |  |  |
| ibias\_ldo\_atb\_0v9\_20ua\_flat | AI | 20uA typical flat current reference from Gbias |
| ibias\_ldo\_atb\_0v9\_20ua\_bgr | AI | 20uA typical Vbg/R current reference from Gbias |
| power\_enable\_atb\_ldo\_0v9 | DI | enable 0.9V LDO |
| set\_vout\_atb\_ldo\_0v9<4:0> | DI | trim bits for 0.9V LDO |
| bypass\_atb\_ldo\_0v9 | DI | bypass 0.9V LDO |
| bypass\_rc\_filter\_atb\_ldo\_0v9 | DI | bypass RC filter |
| ctrl\_decap\_atb\_ldo\_0v9<1:0> | DI | control for decap of 0.9V LDO |
| power\_enable\_atb\_ldo\_1v35 | DI | enable 1.35V LDO |
| bypass\_atb\_ldo\_1v35 | DI | bypass 1.35V LDO |
| **AC ATB signals** | |  |
| enable\_atb\_ac\_pulldwn<16:0> | DI | Pulls down the internal ac channels atb\_ac\_p,n<16:0> to ground |
| atb\_ac\_p<16:0>  atb\_ac\_n<16:0> | AIO | ac channels connecting RX/ WB-ADC/ChirpPLL\_Vtune to ATB internally |
| set\_atb1\_gate\_to\_0v9<17:0> | DI | AC ATB1, connect AC switch gate to 0.9V (biasing) |
| set\_atb1\_gate\_to\_1v35<17:0> | DI | AC ATB1, connect AC switch gate to 1.35V (biasing) |
| set\_atb1\_mid\_to\_vdd<17:0> | DI | AC ATB1, connect AC switch mid to Vdd (biasing) |
| set\_atb1\_mid\_to\_pwell<17:0> | DI | AC ATB1, connect AC switch mid to Pwell (biasing) |
| set\_atb1\_pwell\_to\_vss<17:0> | DI | AC ATB1, connect AC switch Pwell to Vss (biasing) |
| power\_enable\_atb1\_ac\_buf | DI | AC ATB1, power enable IF buffer |
| set\_gain\_atb1\_ac\_buf | DI | AC ATB1, attenuate gain IF buffer |
| enable\_atb1\_ac\_buf\_to\_ext | DI | AC ATB1, enable buffer switches to external |
| enable\_atb1\_ac\_ext\_to\_int | DI | AC ATB1, enable switches external to internal |
| set\_atb2\_gate\_to\_0v9<17:0> | DI | AC ATB2, connect AC switch gate to 0.9V (biasing) |
| set\_atb2\_gate\_to\_1v35<17:0> | DI | AC ATB2, connect AC switch gate to 1.35V (biasing) |
| set\_atb2\_mid\_to\_vdd<17:0> | DI | AC ATB2, connect AC switch mid to Vdd (biasing) |
| set\_atb2\_mid\_to\_pwell<17:0> | DI | AC ATB2, connect AC switch mid to Pwell (biasing) |
| set\_atb2\_pwell\_to\_vss<17:0> | DI | AC ATB2, connect AC switch Pwell to Vss (biasing) |
| power\_enable\_atb2\_ac\_buf | DI | AC ATB2, power enable IF buffer |
| set\_gain\_atb2\_ac\_buf | DI | AC ATB2, attenuate gain IF buffer |
| enable\_atb2\_ac\_buf\_to\_ext | DI | AC ATB2, enable buffer switches to external |
| enable\_atb2\_ac\_ext\_to\_int | DI | AC ATB2, enable switches external to internal |
| **DC ATB signals** | |  |
| atb1\_dc\_[p,n] | AIO | ATB1 shared IP DC bus |
| atb2\_dc\_[p,n] | AIO | ATB2 shared IP DC bus |
| atb1\_dc\_[p,n]\_spare | AIO | TDC ( tempsensor) trim connection |
| atb2\_dc\_[p,n]\_spare | AIO | Spare bus, no connect at RFE top |
| enable\_atb\_dc\_swap | DI | DC ATB[1,2], swap signals @ATB1 to ATB2 AND signals @ATB2 to ATB1 |
| enable\_atb\_dc\_pulldwn<3:0> | DI | DC ATB, pulldown DC testbus to ground (Vssa\_1v8) |
| ctrl\_adc1\_mux\_vp<1:0> | DI | DC ATB1, select input signal for vin[0,2]@ADC1 (pos or neg @ATB) |
| ctrl\_adc1\_mux\_vn<1:0> | DI | DC ATB1, select input signal for vin[1,3]@ADC1 (pos or neg @ATB) |
| ctrl\_adc1\_vneg\_se<1:0> | DI | DC ATB1, select input for VNEG\_SE@ADC1 (Vp, Vn, Vssa\_1v8) |
| ctrl\_adc2\_mux\_vp<1:0> | DI | DC ATB2, select input signal for vin[0,2]@ADC2 (pos or neg @ATB) |
| ctrl\_adc2\_mux\_vn<1:0> | DI | DC ATB2, select input signal for vin[1,3]@ADC2 (pos or neg @ATB) |
| ctrl\_adc2\_vneg\_se<1:0> | DI | DC ATB2, select input for VNEG\_SE@ADC2 (Vp, Vn, Vssa\_1v8) |
| enable\_atb1\_adc\_to\_ext | DI | DC ATB1, connect node adc to node ext |
| enable\_atb1\_adc\_to\_dc | DI | DC ATB1, connect node adc to node dc |
| enable\_atb1\_res0\_to\_dc | DI | DC ATB1, connect node res0 to node dc |
| enable\_atb1\_res1\_to\_dc | DI | DC ATB1, connect node res1 to node dc |
| enable\_atb1\_res0\_to\_adc | DI | DC ATB1, connect node res1 to node adc |
| enable\_atb1\_res1\_to\_adc | DI | DC ATB1, connect node res0 to node adc |
| enable\_atb1\_res0\_to\_ext | DI | DC ATB1, connect node res0 to node ext |
| enable\_atb1\_res1\_to\_ext | DI | DC ATB1, connect node res1 to node ext |
| enable\_atb1\_inout\_to\_adc | DI | DC ATB1, connect node inout to node adc |
| enable\_atb1\_inout\_to\_dc | DI | DC ATB1, connect node inout to node dc |
| enable\_atb1\_inout\_to\_res0 | DI | DC ATB1, connect node inout to node res0 |
| enable\_atb1\_inout\_to\_res1 | DI | DC ATB1, connect node inout to node res1 |
| enable\_atb2\_adc\_to\_ext | DI | DC ATB2, connect node adc to node ext |
| enable\_atb2\_adc\_to\_dc | DI | DC ATB2, connect node adc to node dc |
| enable\_atb2\_res0\_to\_dc | DI | DC ATB2, connect node res0 to node dc |
| enable\_atb2\_res1\_to\_dc | DI | DC ATB2, connect node res1 to node dc |
| enable\_atb2\_res0\_to\_adc | DI | DC ATB2, connect node res1 to node adc |
| enable\_atb2\_res1\_to\_adc | DI | DC ATB2, connect node res0 to node adc |
| enable\_atb2\_res0\_to\_ext | DI | DC ATB2, connect node res0 to node ext |
| enable\_atb2\_res1\_to\_ext | DI | DC ATB2, connect node res1 to node ext |
| enable\_atb2\_inout\_to\_adc | DI | DC ATB2, connect node inout to node adc |
| enable\_atb2\_inout\_to\_dc | DI | DC ATB2, connect node inout to node dc |
| enable\_atb2\_inout\_to\_res0 | DI | DC ATB2, connect node inout to node res0 |
| enable\_atb2\_inout\_to\_res1 | DI | DC ATB2, connect node inout to node res1 |
| set\_res0\_atb1<4:0> | DI | DC ATB1, trim resistor0 (7k8 Ohm) (e.g. 90uA) |
| set\_res1\_atb1<4:0> | DI | DC ATB1, trim resistor1 (35k Ohm) (e.g. 20uA)  (Remark: for 30uA use alternative trim vector and ADC setting, info Benoit Poussard or Lei Ma)" |
| set\_res0\_atb2<4:0> | DI | DC ATB2, trim resistor0 (7k8 Ohm) (e.g. 90uA) |
| set\_res1\_atb2<4:0> | DI | DC ATB2, trim resistor1 (35k Ohm) (e.g. 20uA)  (Remark: for 30uA use alternative trim vector and ADC setting, info Benoit Poussard or Lei Ma)" |
| **RF Buffer** | |  |
| power\_enable\_rf\_buf | DI | enable RF Buffer for chirpPLL\_\_p |
| mcgen\_clk\_chirp\_p | AI | MC Gen clock\_p input ( 2.5GHz) |
| mcgen\_clk\_chirp\_n | AI | MC Gen clock\_n input ( 2.5GHz) |
| chirppll\_lo\_chirp\_p | AI | ChirpPLL VCO divided output clk\_p ( 5GHz) |
| chirppll\_lo\_chirp\_n | AI | ChirpPLL VCO divided output clk\_n ( no Connect internally ) |
| enable\_rf1\_to\_rfint | DI | enable buffer for MCGen\_p |
| enable\_rf2\_to\_rfint | DI | enable buffer for MCGen\_n |
| enable\_rfint\_to\_vss |  | NA |
| control\_spare\_rf\_buf<5:0> | DI | Output power control bits  control\_spare\_rf\_buf<5:4>: for mcgen\_n  control\_spare\_rf\_buf<3:2>: for chirpPLL\_p  control\_spare\_rf\_buf<1:0>: for mcgen\_p |
| **PPD** | |  |
| ibias\_atb\_ppd\_20ua\_bgr | AI | flat 20uA current for PPD bias from GBias ( bgr in pin name is typo, will be changed to flat in ES2 ) |
| power\_enable\_ppd | DI | enable PPD |
| power\_enable\_ppd\_buf | DI | enable PPD buffer |
| power\_enable\_ppd\_vga | DI | enable PPD VGA |
| **REF BIST** | |  |
| power\_enable\_bg | DI | enable Bandgap module |
| ctrl\_bg\_set\_dc<3:0> | DI | trim bits for DC shift @bandgap sub-module |
| ctrl\_bg\_set\_curve<2:0> | DI | trim bits for curvature calibration @bandgap sub-module |
| bg\_bypass\_rc | DI | bypass RC filter post BG module buffer |
| bist\_bypass\_rc | DI | bypass RC filter post BIST reference buffer of |
| power\_enable\_bg\_buffer | DI | enable BG buffer |
| power\_enable\_bist\_buffer | DI | enable BIST buffer |
| mux\_sel\_bist<2:0> | DI | MUX, select bandgap output voltage |
| ibias\_atb\_pvtref\_20ua\_bgr | AI | bgr current from GBias for monitoring/trimming via ATB bus |
| pvtrefgen\_control\_spare<4:0> | DI | spare bits |
|  |  |  |
| **ATB inout external DEBUG pins** | |  |
| atb1\_inout\_[p,n] | AIO | ATB1 Analog Test Bus external pin; 1.8V power domain |
| atb2\_ inout\_ [p,n] | AIO | ATB2 Analog Test Bus external pin; 1.8V power domain |
|  |  |  |
| **ATB INT controls (digital)** | | |
| enable\_bist\_atb1 | DI | enable ATB1 bus connections - used only for the 1HOT coder. |
| enable\_bist\_atb2 | DI | enable ATB2 bus connections - used only for the 1HOT coder. |
| ctrl\_sel\_atb1<24:0> | DI | ATB1 selection (1HOT decoder) |
| ctrl\_sel\_atb2<6:0> | DI | ATB2 selection (1HOT decoder) |
| enable\_bist\_atb\_buf\_in<3:0> | DI | ATB buffer input select (ATB1/2).  Note: Enable either atb1\_<p,n>\_int via buffer OR atb2\_<p,n>\_int via buffer.  bit 0: ATB2  bit 1: ATB1 |
| enable\_bist\_atb\_buf\_out<1:0> | DI | ATB buffer output select (ATB1/2)  bit 0: ATB2  bit 1: ATB1 |
| enable\_bist\_atb\_bypass<1:0> | DI | ATB buffer bypass enable (ATB1/2)  bit 0: ATB2  bit 1: ATB1 |
| enable\_bist\_atb\_vssa<3:0> | DI | Connect IP internal ATB[1,2]\_[P,N]\_INT to local Vssa  bit 0: connect node ATB2\_N\_INT to local Vssa  bit 1: connect node ATB2\_P\_INT to local Vssa  bit 2: connect node ATB1\_N\_INT to local Vssa  bit 3: connect node ATB1\_P\_INT to local Vssa |
| enable\_bist\_atb\_div2<1:0> | DI | Divide-by-2 enable  bit 0: ATB2  bit 1: ATB1 |
| enable\_bist\_atb\_bg\_in | DI | enable, BandGap input to Int ATB |
|  | | |
| enable\_vstress | DI | Enable Voltage Stress mode |
| ctrl\_bg\_vstress\_cycle | DI | BandGap, control voltage stress cycle ('0'==NMOST, '1'==PMOST) |
| **Test signals DfT (digital)** | | |
| xor\_out\_vdda\_1v5\_atb\_\* | DO | DfT functionality, XOR signal(s) for checking Levelshifter(s) @Vdda\_1v5 domain |
| xor\_out\_vdda\_1v8\_atb\_\* | DO | DfT functionality, XOR signal(s) for checking Levelshifter(s) @Vdda\_1v8 domain |
| xor\_out\_vdd\_0v9\_atb\_\* | DO | DfT functionality, XOR signal(s) for checking Levelshifter(s) @Vddd domain |
| xor\_out\_vdda\_0v9\_atb\_\* | DO | DfT functionality, XOR signal(s) for checking Levelshifter(s) @Vdda\_0v9 domain ( from LLDO ) |
| **Spare signals (digital)** | | |
| ctrl\_spare<7:0> | DI | spare logic signal(s) |
| ctrl\_spare2<7:0> | DI | spare logic signal(s) |
| ctrl\_vstress\_spare<1:0> | DI | spare logic signal(s) |

|  |  |  |
| --- | --- | --- |
| **ESD** | | |
| esd\_BOOST |  | Boost pin of ESD clamp , internally connected |
| esd\_TL |  | Trigger line of ESD clamp , connect to TL of other RFE clamps |
| esd\_VDD |  | VDD for ESD clamp |

# General description

## Submodules

RFE ATB top has the following submodules

* LLDO ( Local LDO )
* DC-ATB1, DC-ATB2 (part of *FuSa*)
* AC-ATB1 , AC-ATB2
* RF Buffer ( sometimes called PN Buffer )
* LF PPD ( Peak Power Detector )
* Bandgap Reference ( part of FuSa)
* Local ATB module
* D->A control interface

## DC- ATB

### DCATB- Description

There are 2 DC-ATBs inside RFE ATB. DC ATB is the submodule of ATB for static signals related testing.

It provides infrastructure for sensing static signals from various RFE IPs or for forcing static signals from debug/test pins to IPs. It also has a SAR ADC ( also called ATB(GP)ADC or BIST ADC ) for the purpose of digitizing the static signals.

DC ATB is part of application/mission and Functional Safety(FuSa) and supplied by 1.8V FuSa supply.

As seen in Figure 2 , each DC ATB structurally consists of

* + **CMOS switch matrix (GO2)** - To allow flexible connections between IPs , BIST ADC , and external pins ( pads ATB[1,2]\_[P,N]\_DEBUG )
  + **swap module** ATB[1,2] to ATB[2,1]
  + **2 x (trimmable) Resistors** : for converting currents of interest to voltage quantities
    - [5.1..7.8..10.6]kΩ | step ~180Ω
    - [22..35..47]kΩ | step ~790Ω
  + **ADC (AMSIP) :** SAR ADC
    - modes: diff (11bit) | SE (10bit)
    - Fullscale = 0.8V ( SE ) | 1.6V ( differential )
    - sampling clock (ADC Dig.): [2.5, 4, 5]MHz

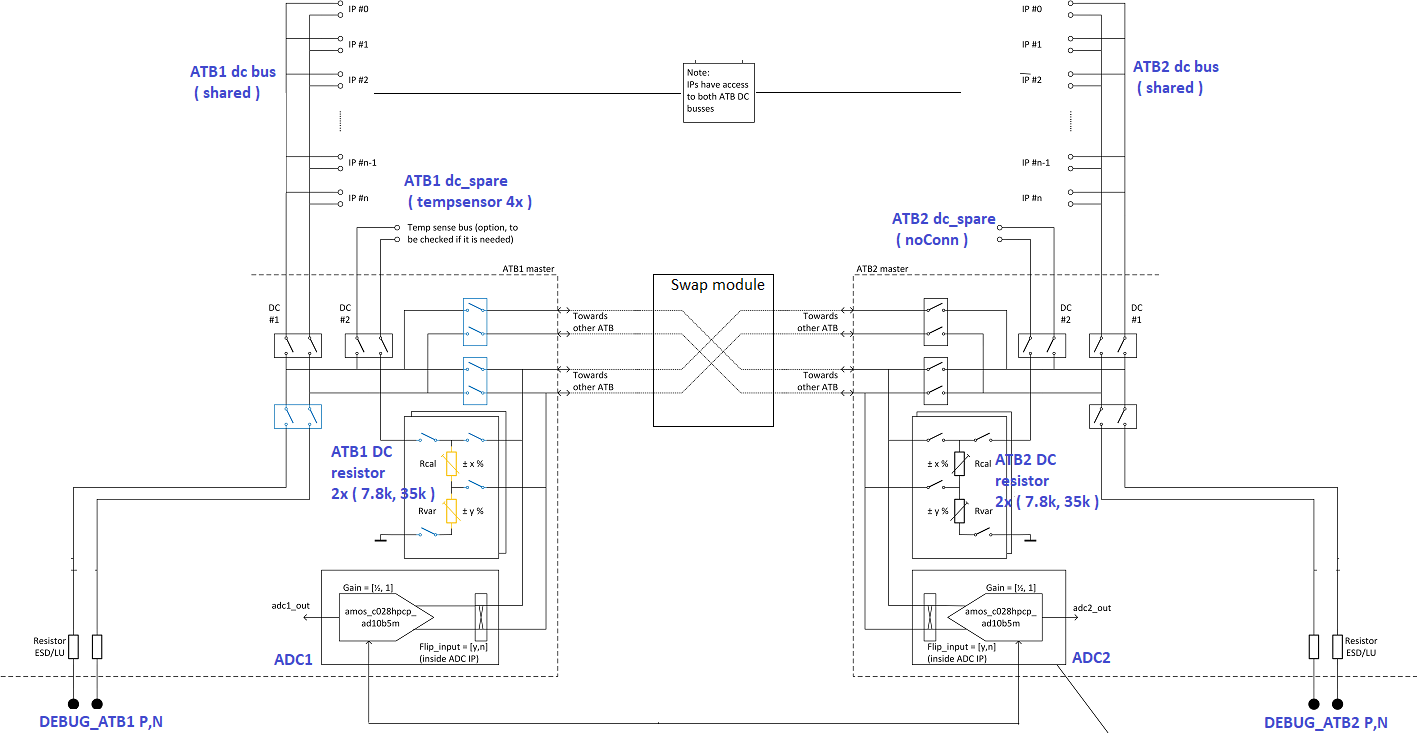


Figure 2. *Simplified Block Diagram of DC ATB*

The various modes of operation of DC ATB is discussed in section 5.3

### DC ATB CMOS GO2 switch

These switches are used to connect an IP to the DC-ATB test bus. Principally, the DC-ATB bus should be connected solely with these switches, to have best visibility on the leakage on the bus, a critical parameter for calibration.

The CMOS T-switch consisting of a NMOS T-switch and a PMOS T-switch in parallel.

NMOS T-switch: Consisting of two NMOS (3 μm/0.25 μm, **nch\_18\_dnw\_mac**) in series, and a small PMOS (**pch\_18\_mac**) that pulls up the middle node in case switch is not conducting. The latter is done to reduce the subthreshold conduction trough the NMOS.

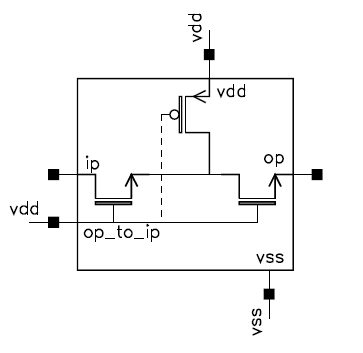


Figure 3 *NMOS T-Switch*

PMOS T-switch Consisting of two PMOS (9 μm/0.25 μm, **pch\_18\_mac**) in series, and a small NMOS (**nch\_18\_dnw\_mac**) that pulls down the middle node in case switch is not conducting. The latter is done to reduce the subthreshold conduction trough the PMOS.

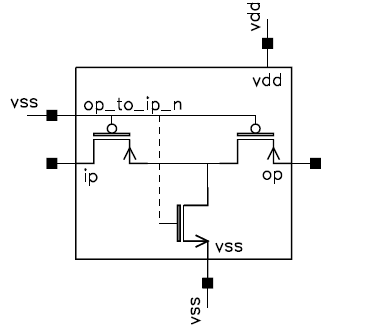


Figure 4 *PMOS T-switch*

The switches are GO2 switches and inside RFE ATB, 1.8V safe supply is used for controlling the ATB switches, because the ATB will be part of a safety mechanism.

The switches have been simulated for three DC parameters:

**Ron** On-resistance: Determined by measuring the voltage drop caused when forcing a 10 μA current through it

**Ileak-on** Leakage current when switch is conducting: Determined by summing the current from ingoing terminal and outgoing terminal, when switch is conducting

**Ileak-off** Leakage current when switch is not conducting: Determined by the current from ingoing terminal when switch is not conducting.

For more details on DC Switch performance , please see [reference 5](#_Referenced_documents).

### DC ATB ADC

The ADC used inside ATB is a third party ( AMSIP ) IP. All the relevant details can be found in the IP datasheet in [reference 4](#_Referenced_documents).

### DCATB- Specifications

Table 2. DC ATB Specifications

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Primary Text** | **Test Min** | **Test Typ** | **Test Max** | **Unit** |
| The ATB1 DC bus and ATB2 DC bus settling time shall be |  |  | 1 | us |
| The value of the first trimmable reference resistor (20uA reference) shall be |  | 35k |  |  |
| Resistance range of the first trimmable reference resistor shall be | 22 | 35 | 46 | kOhm |
| Value of the second trimmable reference resistor (90uA reference) shall be |  | 7.8 |  | kOhm |
| Resistance range of the second trimmable reference resistor shall be | 5.1 | 7.8 | 10.6 | kOhm |
| The DC switches voltage range shall be |  |  | 1.8 | V |
| The DC swiches shall have a switch ON resistance of |  |  | 4 | kOhm |
| The DC swiches shall have an absolute switch ON leakage |  |  | 50 | nA |
| The DC swiches shall have an absolute switch OFF leakage (over the full voltage range) |  |  | 100 | nA |

### DCATB- Performance

Please check ATB design review - <https://www.collabnet.nxp.com/sf/go/doc521556?nav=1&pagenum=1&pagesize=15>

## AC ATB

### AC ATB Description

There are 2 AC-ATBs inside ATB. AC ATB is the submodule of ATB providing the infrastructure for IF/baseband signals ( freq<40MHz) related testing. The use cases include sensing baseband/IF (<40MHz) signals from RX or for forcing baseband signals from debug/test pins to RX

AC ATB is part of characterization test/validation. As seen in figure 5 , each AC ATB is fully differential and structurally consists of

* + **NMOS switch matrix** (GO1, and GO2)
  + **IF/AC Buffer** (incl. powerdown)

The NMOS switch matrix has –

1. 17 (GO1) ac switches , one per channel , SW1 in fig 5
2. buffer input GO1 ac switch , SW2 in fig 5
3. external <-> internal GO2 switch ( to bypass the buffer ) , SW3 in fig 5
4. buffer output -> external GO2 switch, SW4 in fig 5

Externally, the AC ATB interfaces with the DEBUG\_ATB1 [P,N] and DEBUG\_ATB2 [P,N] pins ( the same pins external pins as DC ATB )

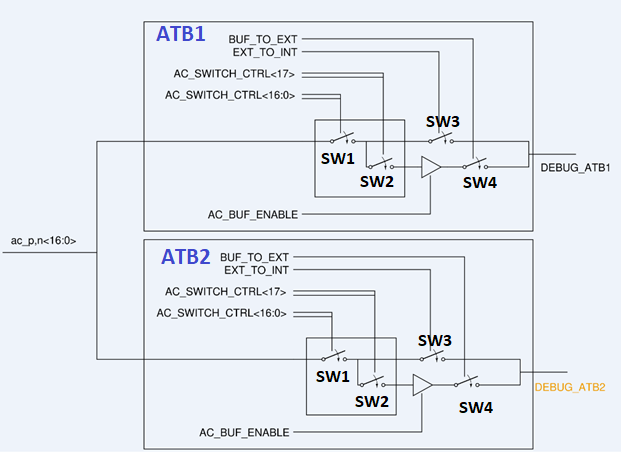


Figure 5 AC ATB simplified construction

Various modes of AC ATB operation are discussed in section 5.4

### ACATB Switch

Each ac channel inside AC ATB is controlled by a dedicated ac switch ( SW1 in Fig 5 ) , the construction of which is shown as in figure 6.

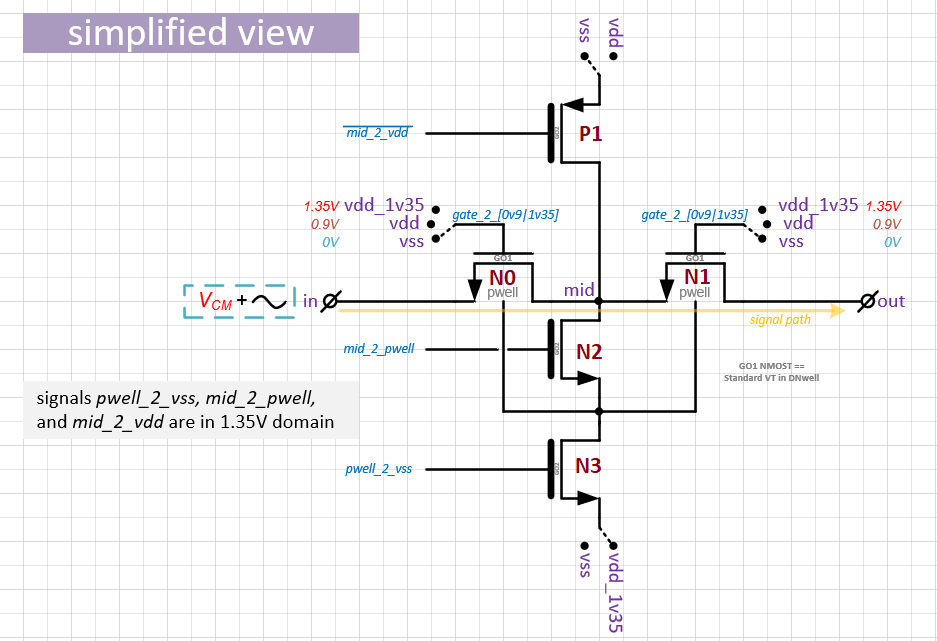


Figure 6 AC ATB channel switch

Two GO1 NMOS in series ( N0, N1 ) are the ‘switch’ part. The core or base operating voltage for the technology is 0.9 Volts +/- 10%. This voltage is the nominal voltage for all low voltage devices (thin oxide devices). The device should be designed for a +10% to -10% voltage variation from the nominal 0.9 volts. In order to obtain high linearity from these switches, N0,N1 gates can be controlled by 1.35V internally ( LLDO ) generated supply as well ( in addition to 0.9V control ) . However, in order to avoid stressing the thin oxide MOS devices, it is recommended to follow ac switch sequencing as explained next.

P1, N2, N3 are GO2 MOS for defining the mid node of N0,N1 and their respective pwells appropriately in ON and OFF states.

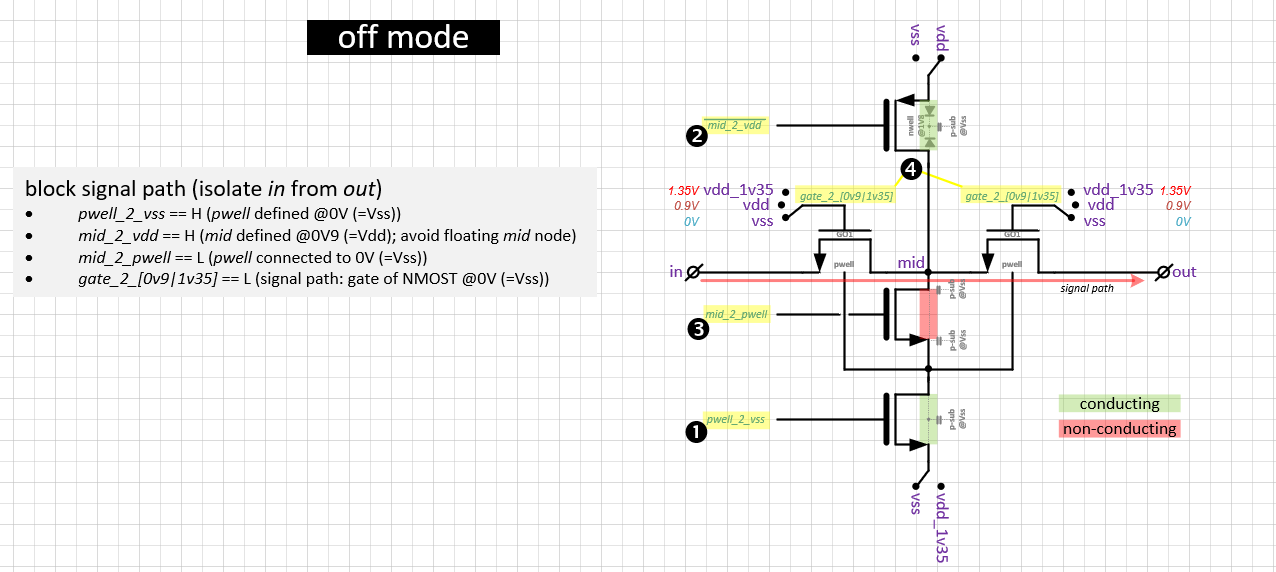
### AC switch control sequencing

As mentioned, the gates of N0,N1 in Fig 6 can be at 0.9V or 1.35V ( which is high linearity mode ). It is assumed that the switches will be operated in high linearity mode for all practical purposes. Since there is no mechanism internally which prevents GO1 devices from stress on exposure to 1.35V , it has to be ensured from proper sequencing of gate controls in validation as described below.

Depending on the channel(s) needed to be turned on , for the corresponding switch, turn on sequence should be

***OFF-> 0v9 mode-> ac signal application -> 1v35 mode***

#### AC switch in OFF mode

Figure 7.*OFF mode of AC switch*

#### AC switch in 0v9 mode

Figure 8. 0v9 mode of AC switch

#### AC switch in 1v35 mode

Figure 9. 1v35 mode of AC switch

### AC ATB Specifications

All the specifications below are including routing parasitics , RX load , and external loading ( cable , acquisition equipment ,etc. )

Table 3. AC ATB Specifications ( considering all routing parasitics and RX load )

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Primary Text** | **Test Min** | **Test Typ** | **Test Max** | **Unit** |
| The bandwidth (-3dB) of the AC\_ATB path between the IC balls and the IF output of the connected receiver (RX1...RX4) shall be | 60 |  |  | MHz |
| The linearity (oip3) of the signal path from the RX outputs to the ATB IP outputs shall be better than | 17 |  |  | dB |
| The image rejection ratio (IRR) between I & Q signals path from a receiver output to the ATB output shall be |  |  | 40 | dB |
| The equivalent Noise Floor of the AC\_ATB at the IF output / ATB input interface shall be |  |  | -140 | dBm/Hz |
| The gain difference between the all the different RX AC\_ATB paths to the ATB outputs shall be |  |  | 0.1 | dB |
| The phase difference between all the different RX AC\_ATB paths to the ATB outputs shall be |  |  | 1 | degree |
| Bandwidth (-3dB) of the AC\_ATB signal path to the RX-ADC IP. | 60 |  |  | MHz |
| The linearity of the signal path from the external ATB balls to the RX-ADC IP inputs, for signals in the 0-40MHz frequency range with a maximum amplitude of 1.2Vppdiff, shall be | 80 |  |  | dBc |
| The IF analog buffer input voltage shall be |  |  | 1.2 | Vpk-pk |
| The IF analog buffer shall have a compression point higher than |  | 0 |  | dBm |
| The isolation between two IF analog buffers shall be | 40 |  |  |  |
| The IF analog test buffer shall present a broadband behaviour (-3dB cutoff) such to not degrade transfer function of RX blocks being measured of | 60 |  |  | MHz |
| The IF buffer current consumption shall be less than |  |  | 25 | mA |

### AC ATB Performance

Please check ATB design review - <https://www.collabnet.nxp.com/sf/go/doc521556?nav=1&pagenum=1&pagesize=15>

## RF Buffer

### RF BUFFER Description

RF Buffer provides the means to bring out GHz signals from Master Clock Generator (a.k.a. XO ~ 2.5GHz) and Chirp PLL VCO ( Divided version , 5GHz) for PhaseNoise ( PN) measurement. RF Buffer is part of characterization, production testing. RF Buffer performance is verified for 2GHz-6GHz signals.Overall, there are three buffers inside RF buffer block

2xbuffers for MCGEN clock is p and n (symmetric loading)

1x buffer for ChirpPLL VCO ( div/2) : only p is buffered

termination resistor - drain with 50Ω (on chip) in series to local supply of RF Buffer ( from ATB LDO )

RF Buffer connects to PLL\_TEST pad output.

### Buffer for 5 GHz ChirpPLL VCO( freq. div/2 ) out

The chirpPLL p signal is buffered through a series of inverters. ( The n signal is terminated with a dummy stage to maintain balanced load to the differential output from ChirpPLL). Powerdown feature is added to input stage. The output power is 2 bit programmable and buffer output is internally terminated by 50 ohm resistor.

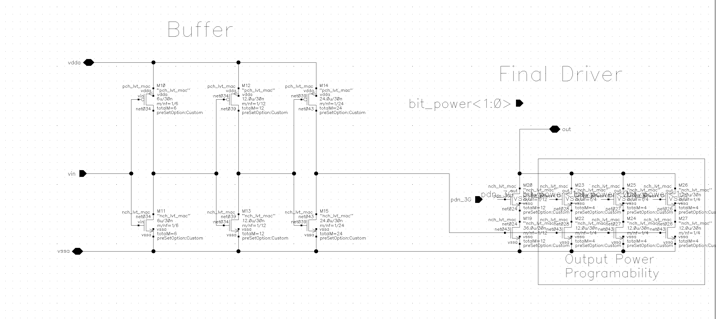


Figure 10. *RF Buffer ( 5G ) schematic*

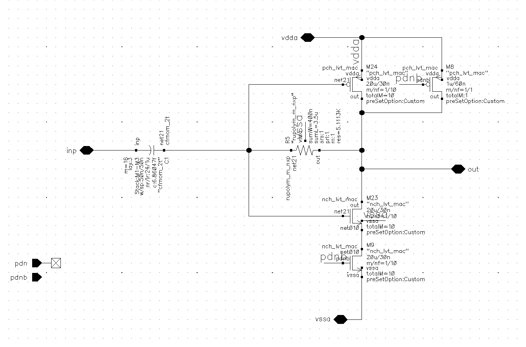


Figure 11. *RF Buffer (5G) input stage*

### Buffer for 2.56 GHz ClockPLL out

The clockPLL p and n signal is buffered through a series of inverters. Powerdown feature is added to output stage of the first inverter. The output power is 2 bit programmable and buffer output is internally terminated by 50 ohm resistor.

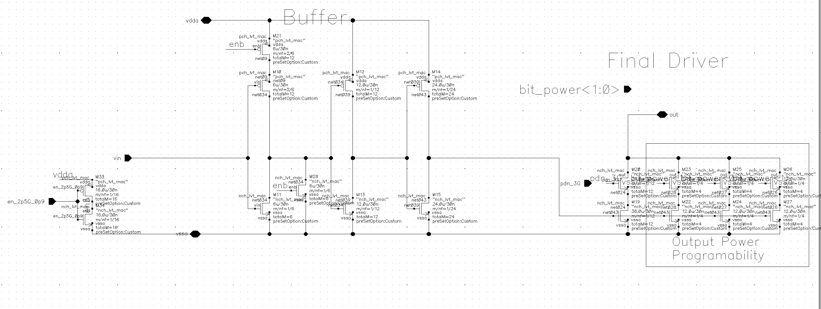


Figure 12. *RF Buffer ( 2.5G ) schematic*

### RF BUFFER Specifications

Table 4 . RF Buffer specifications

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Primary Text** | **Test Min** | **Test Typ** | **Test Max** | **Unit** |
| The HF buffer for PN test shall operate in the range | 0.32 | 5 | 6 | GHz |
| The HF buffer for PN test output power shall be in the range |  |  | -8 | dBm |
| The HF Buffer PN spec at 10kHz freq offset and for a 5GHz output shall be |  |  | -120 |  |
| The HF Buffer PN spec at 100kHz freq offset and for a 5GHz output shall be |  |  | -130 |  |
| The HF Buffer PN spec at 1MHz freq offset and for a 5GHz output shall be |  |  | -140 |  |
| The HF Buffer PN spec at 10MHz freq offset and for a 5GHz output shall be |  |  | -150 |  |
| The HF buffer current consumption shall be less than |  |  | 25 | mA |

### RF BUFFER Performance

Please check ATB design review - <https://www.collabnet.nxp.com/sf/go/doc521556?nav=1&pagenum=1&pagesize=15>

## PPD

### PPD Description

PPD function is to allow monitoring of the power levels of the RF signals through RF buffer or external pll\_test pin. PPD converts the amplitude information to a static quantity which is then measured via the DC ATB.

### PPD Specifications

### ATB- PPD Performance

Please check ATB design review - <https://www.collabnet.nxp.com/sf/go/doc521556?nav=1&pagenum=1&pagesize=15>

## Bandgap Reference ( for ATB ADC )

### ATB ADC BGR

ATB ADC BG is the bandgap module C028HPCP\_BG0V9 , which provides 0.7V typ reference voltage to the BIST ADC of DC ATB. It also allows access to multiple level voltage taps which are used for BIST ADC calibration.

### ATB ADC BGR Specifications

Please refer to Bandgap IP datasheet [, Ref.1](#_Referenced_documents)

## LLDO

### LLDO Description

ATB Local LDO is the modular 0.9V LDO with output current capability of 27mA .This 0.9V LDO forms the reference for the next stage that generates the 1.35V local supply. The 0.9V supply is used by AC ATB (switches and IF buffer) , RF Buffer , PPD ( either IF or RF section active at a time ). The 1.35V supply is used by AC ATB switches.

### LLDO Specifications

### LLDO Performance

## INTERNAL ATB

### INTERNAL ATB Description

Internal ATB module provides the feature to connect ATB internal nodes of interest on atb1/2\_p/n\_int nets below ( for eg. from output of REF BIST , LLDO , PPD,etc ) to the DCATB module with extra features like buffering or div by 2 internally.

|  |
| --- |
|  |

Figure 13. simplified internal ATB block diagram

# Functional description

## Basic functions

Broadly speaking , ATB provides the infrastructure for testing and trimming of RFE IPs , by providing necessary connectivity to and from the external test environment. ATB ; specifically the DC ATB ( and ATB ADC BG ) are part of mission mode due to their involvement in monitoring IP LLDO levels in field.

The external DEBUG\_ATB pads are shared between DCATB, ACATB – so only one route can be active when using them, i.e. one can NOT perform external DC or external IF measurements , both at the same time.

Additionally, AC ATB and RF Buffer, PPD use the same internal LLDO for supplies , and at a time either the IF(baseband) or the RF subsection should be active from ATB point of view. One should NOT perform Phase noise ( via RF buffer ) and IF ( via AC ATB ) measurements at the same time.

## Startup

ATB IP starts up when pon\_ls\_atb (PowerON\_LevelShifter) from digital core goes high.

All digital interfacing with the ATB analog domain goes via levelshifter modules which are part of ATB interface. These levelshifters are controlled by the digital core by means of signal *pon\_ls\_atb* . As long as signal *pon\_ls* is low, the levelshifters are blocking the signal flow from the digital domain to the analog domain. This prevents unwanted behavior in the analog domain while the digital core is (still) starting up and digital signals are not defined yet. During startup of the RFE signal *pon\_ls* is initially controlled by the analog domain and forced to 0V. Once the digital core is active signal *pon\_ls* will be controlled via the digital domain.

While *pon\_ls* is logic state ‘0’, the (analog) output of the levelshifter can be forced to 0V or track the Vdda supply. The latter means that when Vdda is ramped up the output of the levelshifter represents a logic state ‘1’ in the analog domain. The two different states are reflected in the following schematic views:

* ida\_mmw\_rfe\_shared\_levelshifters\_lib/ls\_up\_w\_xor\_def0\_sep
  + output is defined at 0V while pon\_ls is ‘0’
* ida\_mmw\_rfe\_shared\_levelshifters\_lib/ls\_up\_w\_xor\_def1\_sep
  + output is defined at *Vdda* V while pon\_ls is ‘0’

To guarantee proper startup of the ATB the crucial/relevant bit settings are hardcoded via the levelshifters, for example *atb pulldowns*.

## DC ATB Operation

DC ATB interfaces with multiple RFE IPs . It is part of production test , and FuSa in application ( mission mode ).

Internally, the DC bus consists of ATB1 dc\_[p,n] and ATB2 dc\_[p,n] which is shared bus between multiple IPs in a non-conflicting manner.

ATB1 dc\_[p,n]\_spare is a star connect of the ATB1 dc\_[p,n] bus which is connected to the RFE 4x tempsensors ( also called TDC ) vtrim nodes.

DC ATB externally interfaces with DEBUG\_ATB1 and DEBUG\_ATB2 pins.

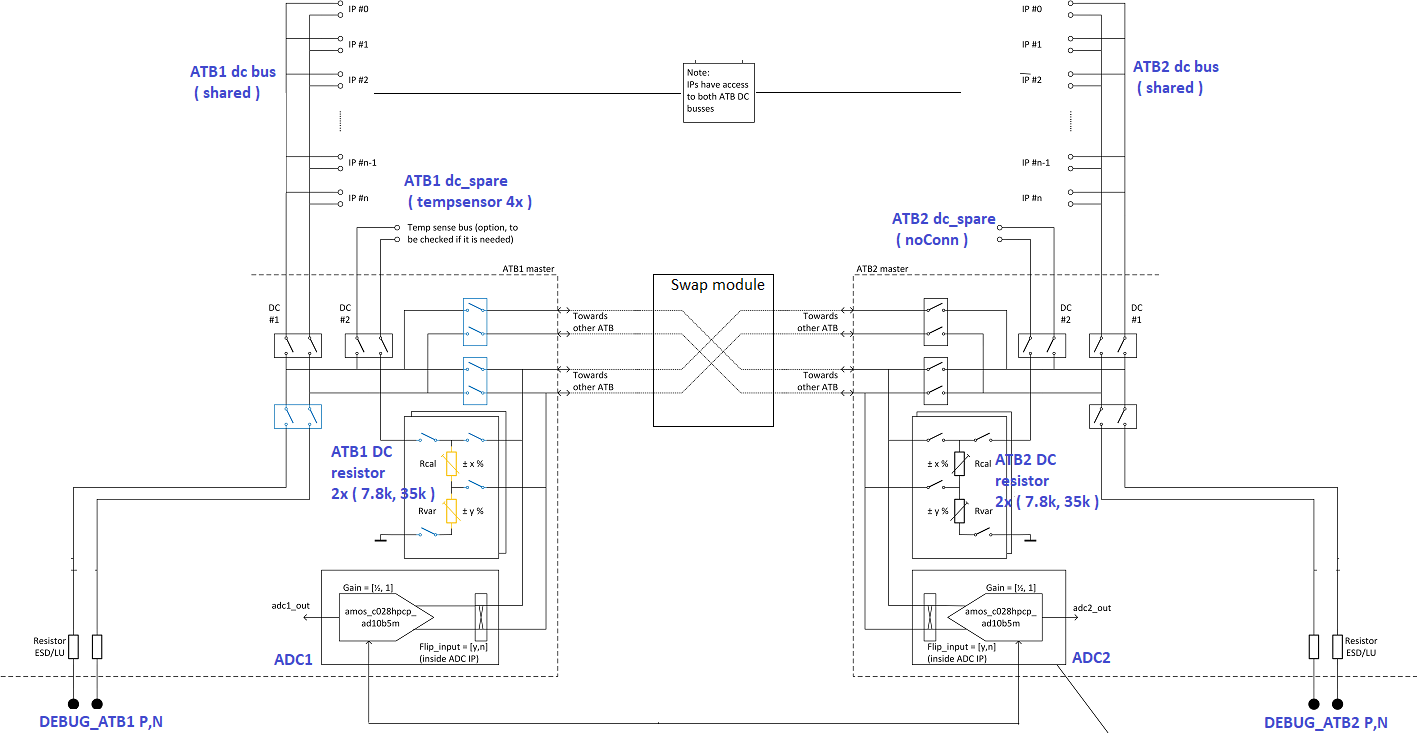


Figure 14. *Simplified diagram of DC ATB*

It is very important to avoid ATB DC Bus conflicts, i.e. multiple IPs driving DC ATB at the same time.

Each RFE IP connected to the ATB uses local controls to determine the 1-HOT coded subIP selectors.

Each RFE IP also uses an enable from the SPIM to close the switch from the IP towards the ATB. The SPIM can then ensure that also the IPs never have any conflicts on the bus.

So, the local ATB<x>\_EN inside the RFE IP is used only for the 1HOT coding, and does not enable the IP switch. You need both the IP enable and the enable from the SPIM to connect to the ATB bus.

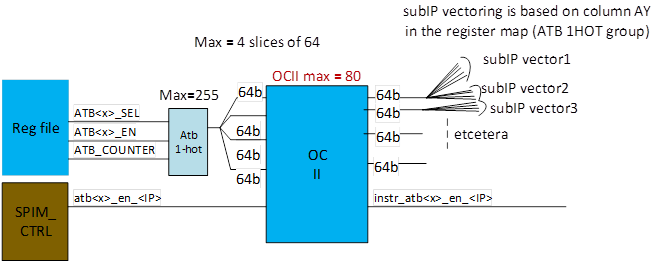
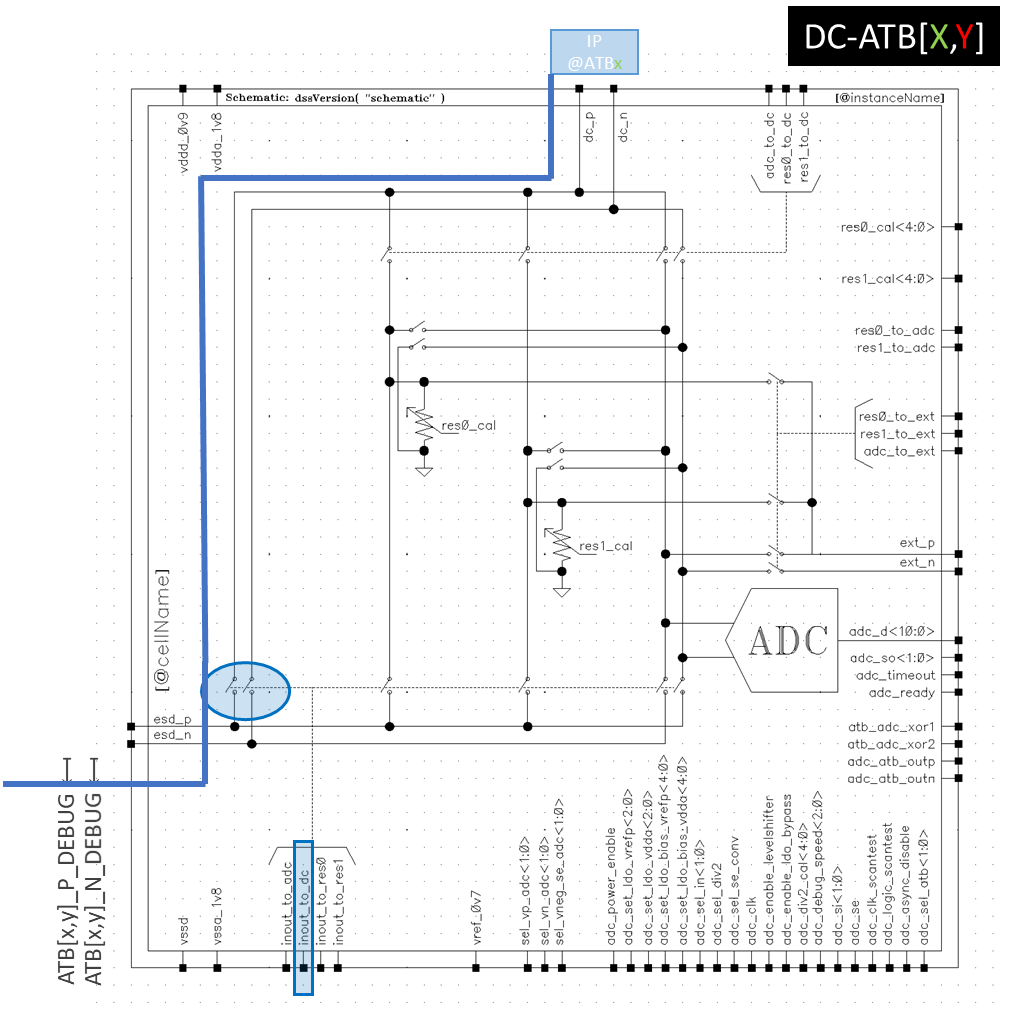


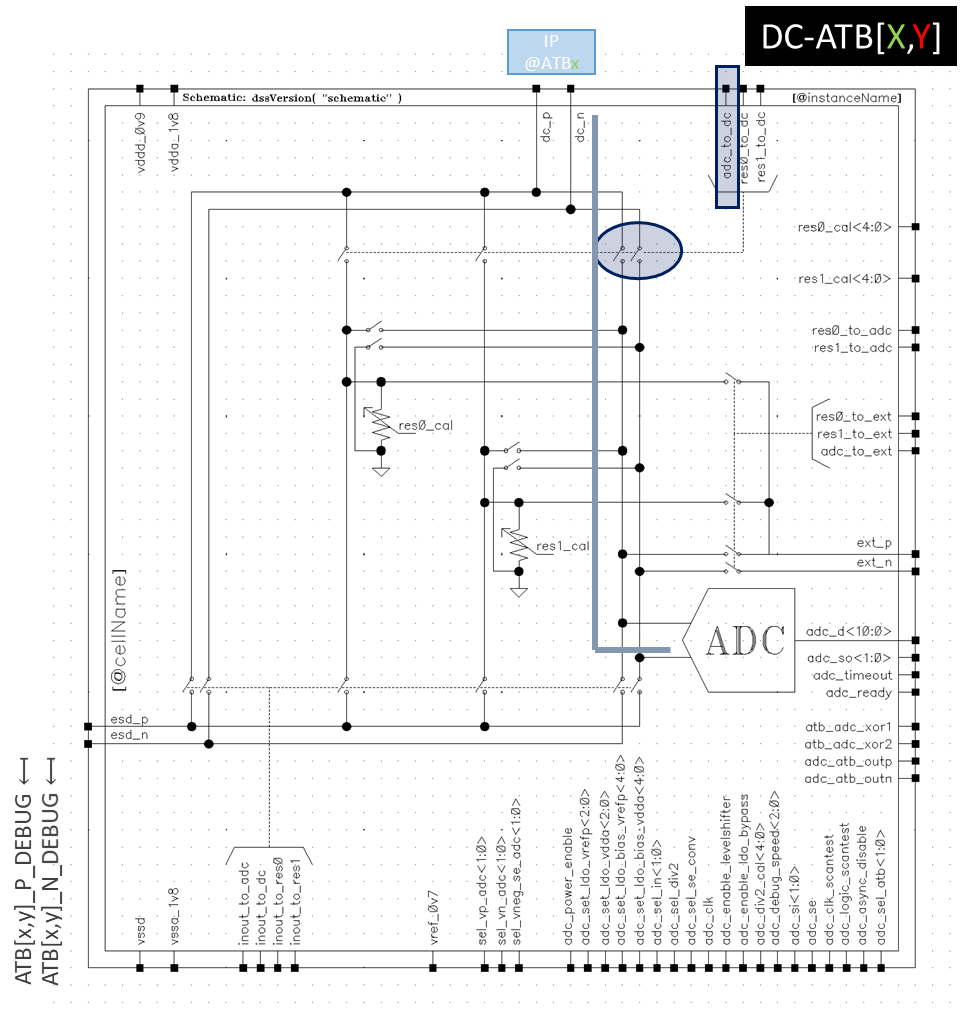
Figure 15. ATB BUS 1-Hot control from digital

The major connectivity modes of DC ATB are activated by means of turning on appropriate switches ( described in [section 4.2.2](#_DC_ATB_CMOS)) as illustrated in the following figures ( the switch control names are boxed in color in the figures ).

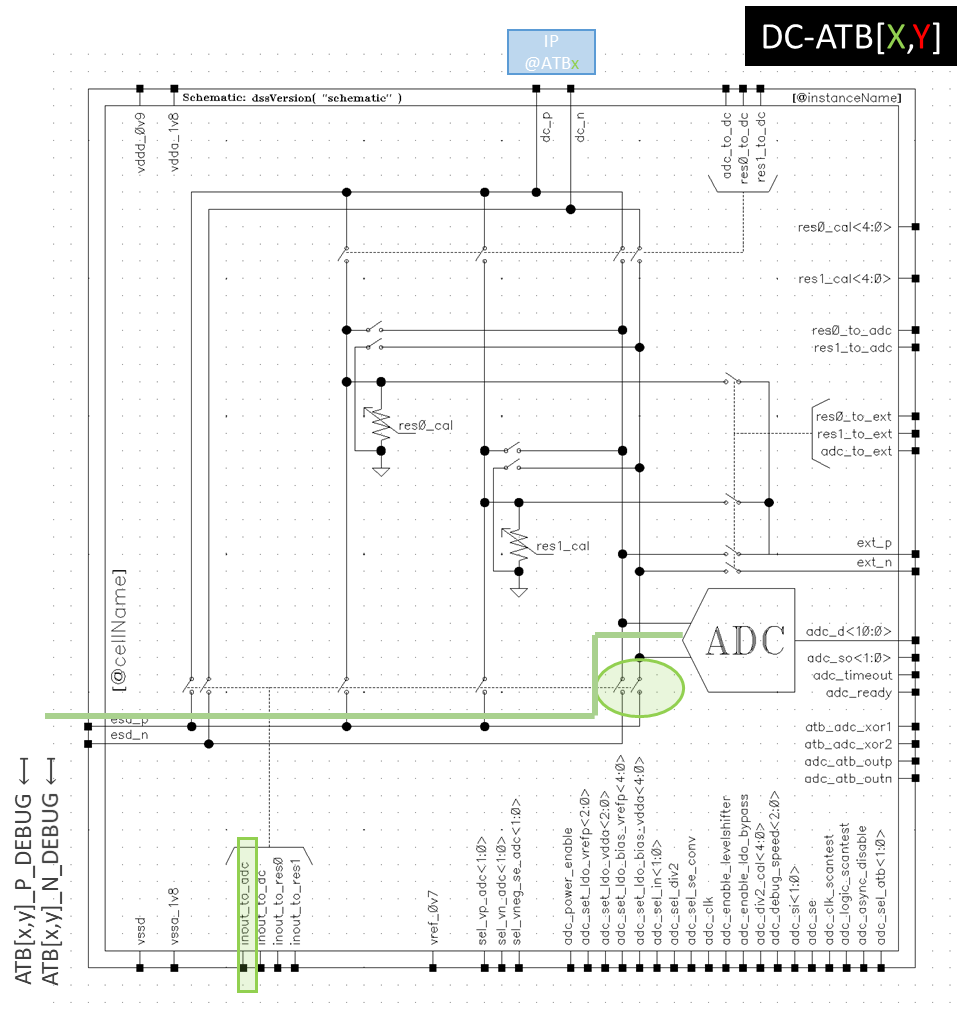
**<i> IP -> external & external -> IP**



**<ii> IP -> ATB(GP)ADC**

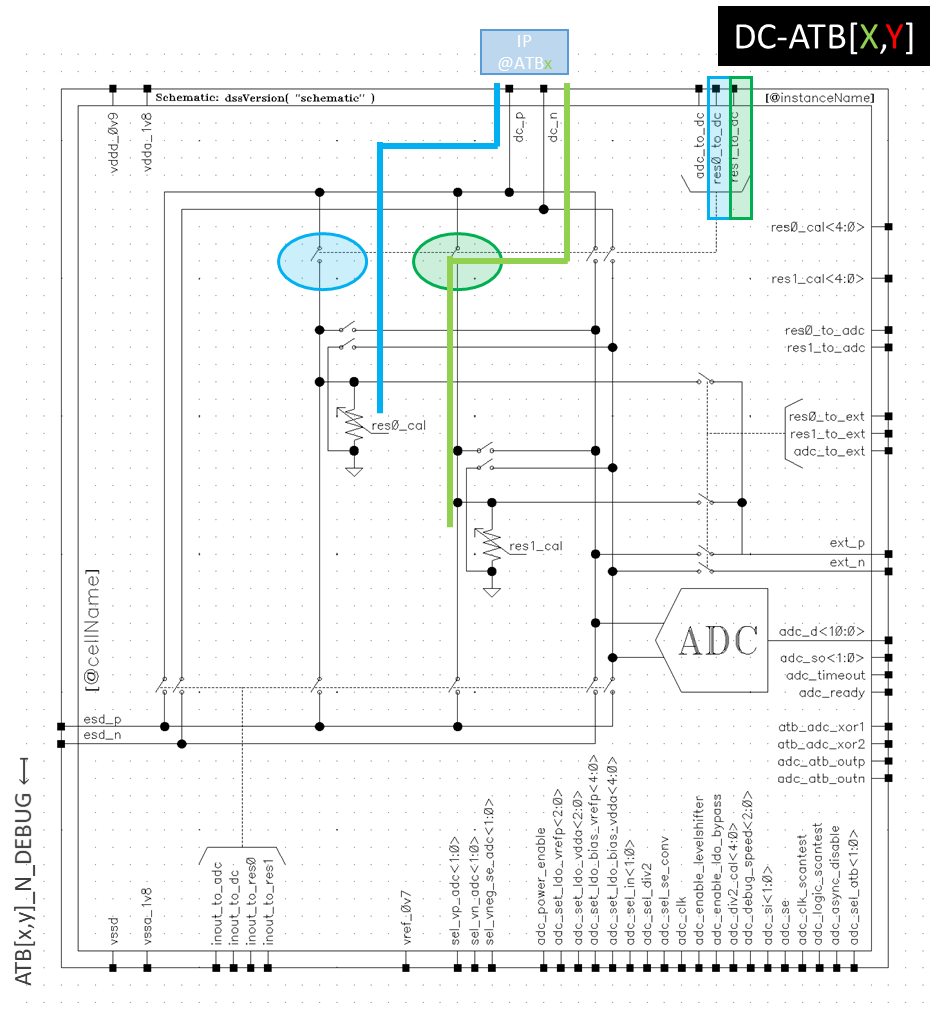


**<iii> External -> ATB(GP)ADC**

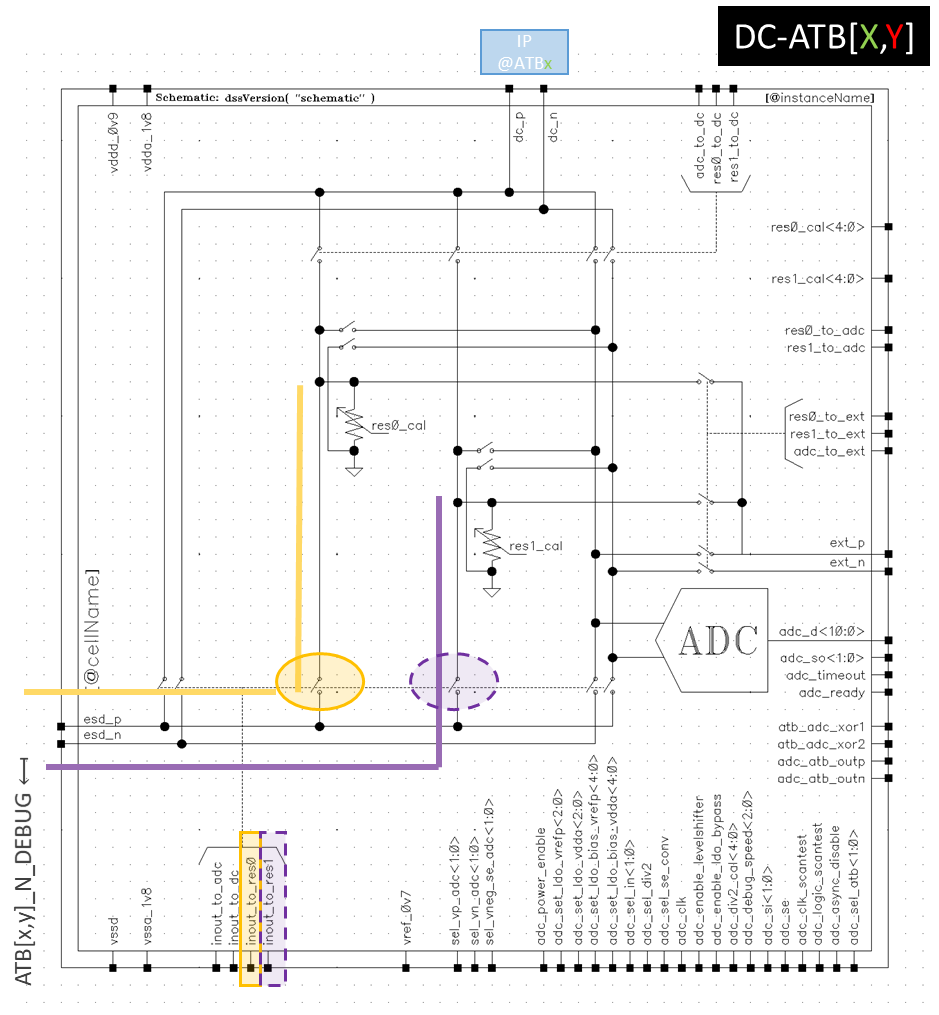


**<iii> IP( current ) -> DCATB resistor**

There are two 5-bit trimmable resistors inside DC ATB. res0 – 7.8kohms for 90uA currents , res1 – 35kohms for 20-30uA currents . Once current is pumped into the appropriate resistor , the resultant voltage can be routed to either the ATB-ADC ( res0\_to\_adc , res1\_to\_adc switches ) or external DEBUG pins(res0\_to\_inout , res1\_to\_inout switches )



**<v> External ( current ) -> DCATB resistor**



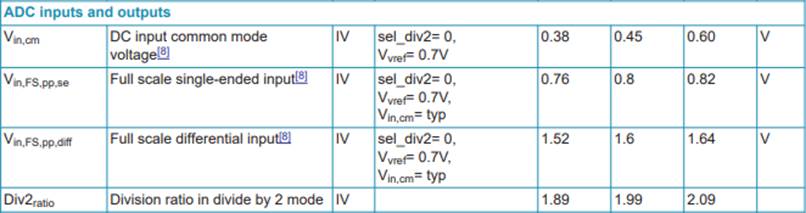
Trimming strategy document can be found in [Ref 6.](#_Referenced_documents)

### IP potentials monitored via ATB ADC

One of the main use cases of DC ATB is monitoring of IP node potentials of interest on DC bus via the BIST ADC. For example, in FuSa routine , various IP LLDO potentials are checked for overvoltage undervoltage levels.

There are a few options provided for configuring proper signal and ground level from IP to ATB ADC

The ADC can be used in Single ended ( SE ) or differential mode , with the following specs on voltage levels –



Prior to being fed to ADC , there is a MUX tree inside ATB which provides flexibility in configuring the ADC input and ground potentials.

#### ADC in Differential mode

The MUX tree input potentials ( vp\_adc , vn\_adc ) come from the shared dc bus ( atb dc\_p , atb dc\_n ). IPs can provide their differential signals of interest on the bus . The VP, VN MUX tree allows the flexibility to feed the IP output to ADC input with and without change in polarity( p,n swap ).

|  |
| --- |
| More details on the MUX tree can be found in the ticket (  ***[ATB-RFE] possibility to cancel offset by swapping so-called p- and n-signal at DC-ATB*** |
|  |

<https://www.collabnet.nxp.com/sf/go/artf825496> )

In Fig. 16 : a 3-input-MUX is introduced which makes it possible to swap nodes *vp\_adc* and *vn\_adc* going to the ADC:

*vp\_adc* ↔ pos. input *vin\_adc<0>* (\*)

OR neg. input *vin\_adc<3>* (\*)

*vn\_adc* ↔ neg. input *vin\_adc<1>* (\*)

OR pos. input *vin<adc<2>* (\*)

The T switches in the MUX are implemented as NMOS or CMOS (NMOS||PMOS) and

the middle (T) node is pulled to *ground*@PMOST and pulled to *supply*@NMOST.

The choice for pulling the T-node to ground or supply is based on not having any logic within the cells (i.e. optimize layout)

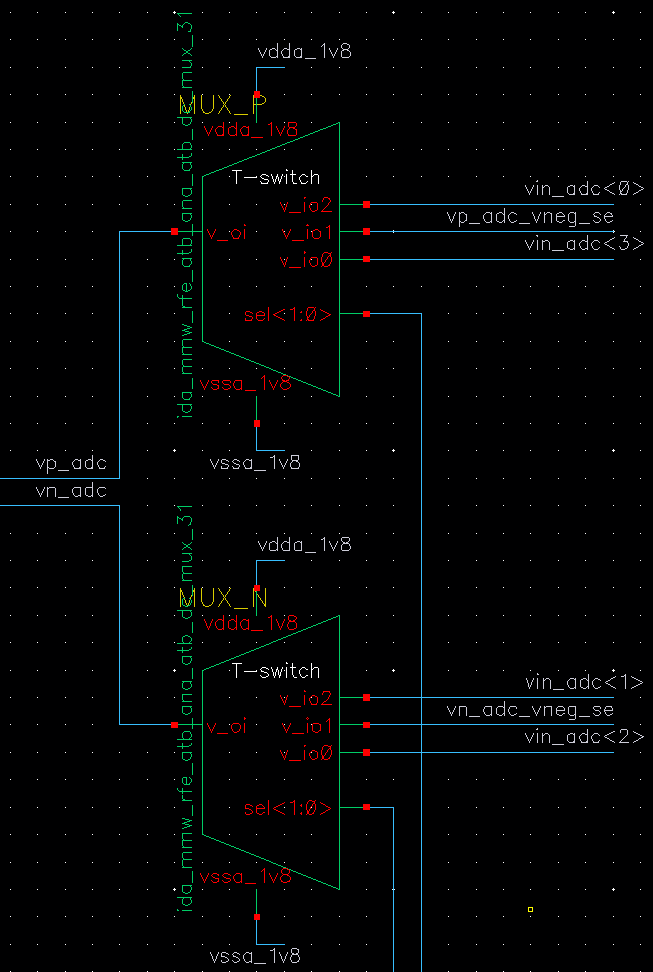
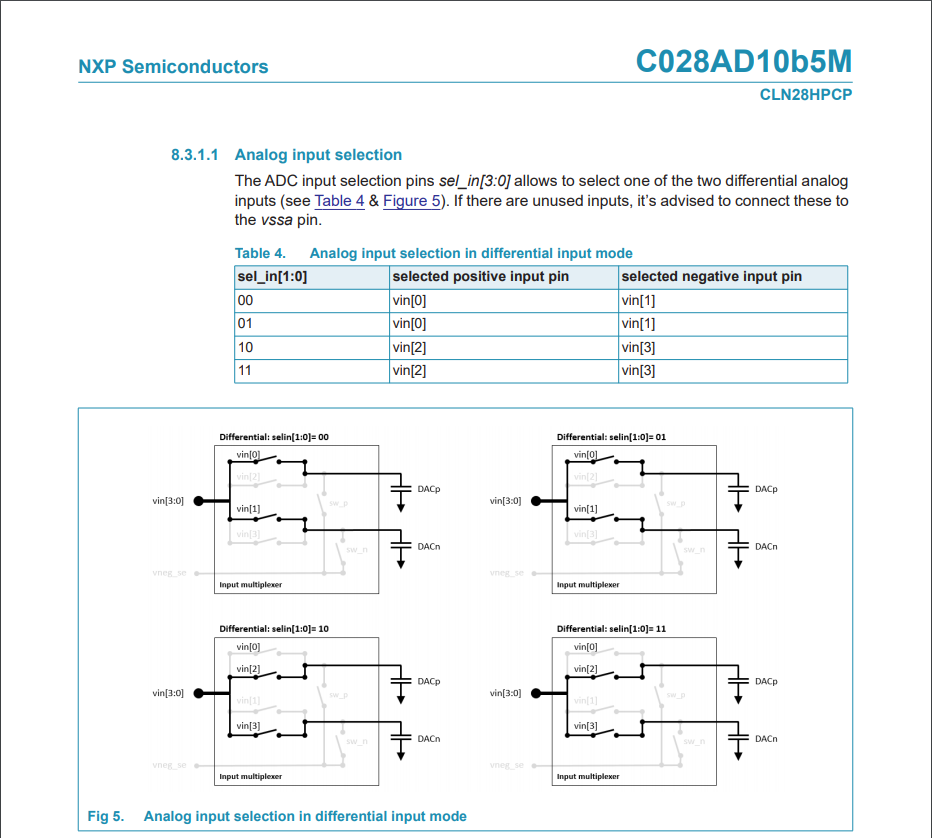
 

Figure 16. MUX tree input before ATB-ADC

#### ADC in SE mode

In SE mode , the ADC input is measured with respect to the potential on its vneg\_se terminal. Inside ATB , vneg\_se can be configured to be one of the following

<i> ATB local ground ( vssa\_1v8 )

<ii> Vp ( or atb dc\_p node )

<iii> Vn ( or atb dc\_n node )

Most IP will put the ref. ground on the *atb\_n* and the voltage to be measured on the *atb\_p.*

In case an IP puts e.g. the ref. ground on the *atb\_p* and the voltage to be measured on the *atb\_n*. Then use the MUX\_P and MUX\_N to swap the *atb\_p* and *atb\_n* connection to the ADC and properly configure vneg\_se as per need.

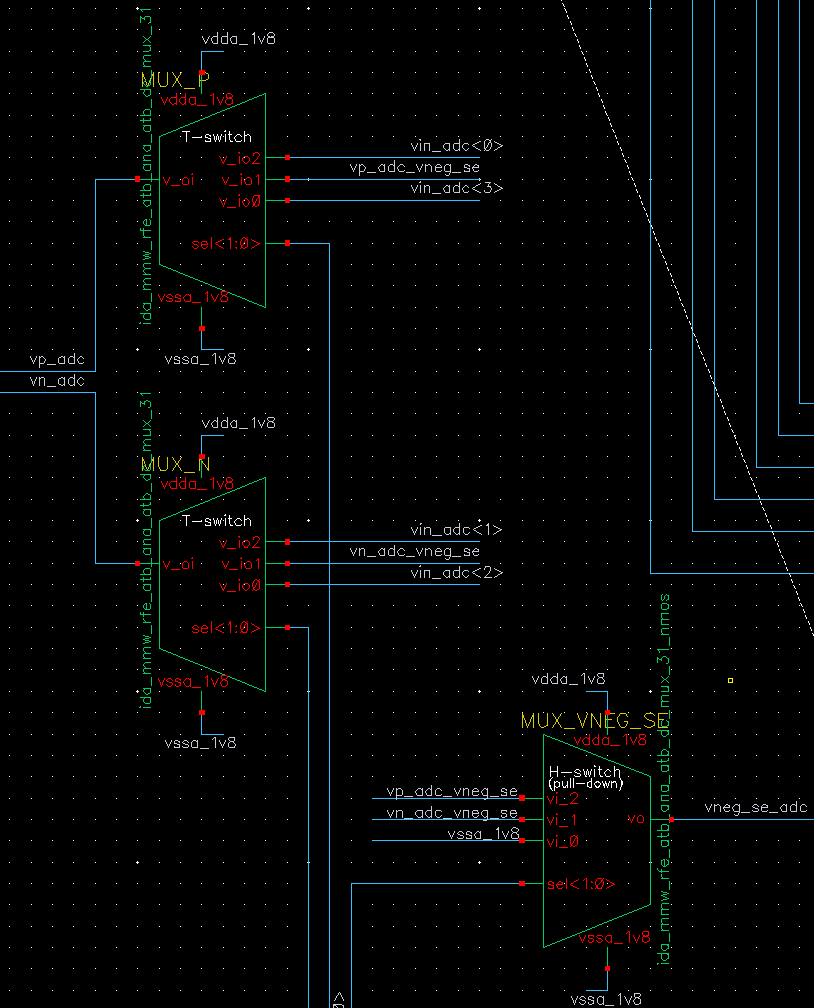
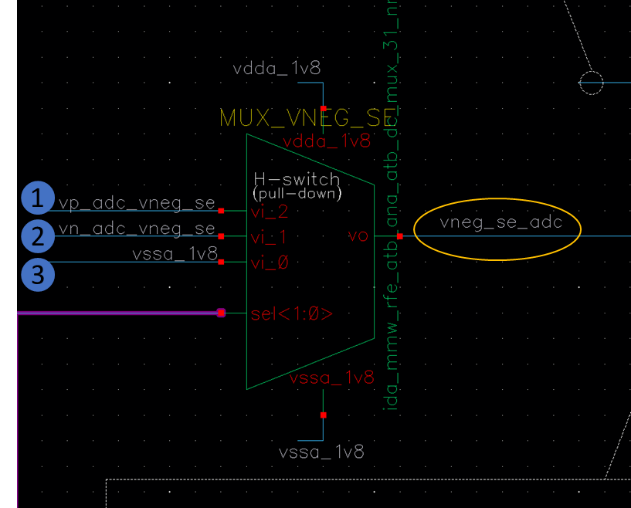
 

Figure 17. Selection for Vneg\_SE potential in ATB\_ADC single ended mode

More information about this feature is captured in ***([RFE\_DFT\_ATB]Add extra switch control to vneg\_se signal in BISTADC block*:** <https://www.collabnet.nxp.com/sf/go/artf813571>)

Another point of measuring SE potentials of the IPs , is that most IP reference voltages to be measured are with respect to their local reference ground. As such, one wants to measure the difference between the 2 IP nodes via SE@ADC. Therefore, ATB facilitates sending the IP reference ground over the *atb\_n* along with the signal on the *atb\_p*. However, the voltage tolerance on the *vneg\_se*@ADC is roughly <100mV. When the voltage on *vneg\_se* >100mV , the value coming out of the ADC is most likely not representative or accurate enough for the voltage difference @IP. For this purpose:

* The local *vssa\_1v8* was introduced. This opened a 3-step approach for measuring the voltage difference @IP:

1. Measure the signal on the *atb\_p* referenced to the *vssa\_1v8*.
2. Measure the signal on the *atb\_n* referenced to the *vssa\_1v8*.
3. Take the difference between 1. and 2.

### DC-ATB-Tempsensor connections

STRX has 4 Temperature-to-Digital converters ( also called TDC or tempsensor ). The TDCs need to be trimmed via external voltage on ATB and since there is a strict requirement on accuracy of the TDC trim ( 1 degree or lesser ) , it helps to have a dedicated dc bus from the external ATB pins to the tempsensor IPs , so that the trim voltage does not suffer from IR drop due to leakage from off switches of other IPs connected to the shared DC bus.

#### ES1/ES1-Mfix connections between ATB and TDC

The DCATB towards IP side have two sets of differential pins. DC\_p/n ( shared DC bus for all IPs ) and DC\_spare\_p/n. The DC\_spare connections go towards the 4xTDC. In design , the two sets of pins are star connected , so there is no real isolation between the shared DC bus ( DC\_p/n) and the TDC bus ( DC\_spare ).

This configuration does not create much accuracy loss as such , since the leakage current from off switches of shared DC bus is a small number. However, it did lead to another major issue in ES1 as described ahead.

The DC\_spare\_p/n connect to vtrimp,vtrimn pins of the TDC IP. Internally, the TDCIP grounds its vtrimn pin to its local ground/vssa for improving the trimming accuracy. And because the vtrimn is connected to DC\_spare\_n , which in turn is star connected to DC\_n bus, the entire DC shared bus n side gets grounded via the TDC. This configuration is illustrated in red line in figure 18.

.

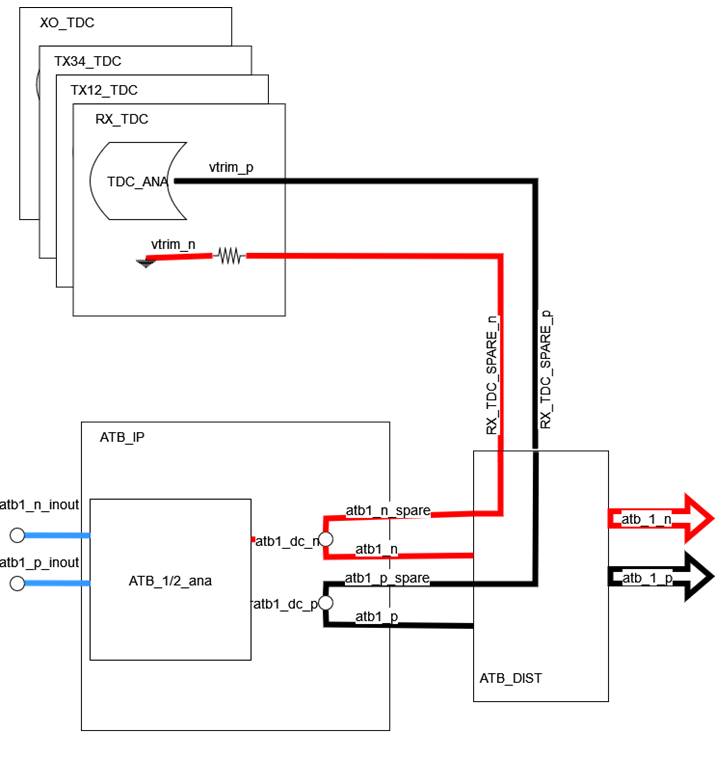


Figure . ATB-TDC connections in ES1

This issue was fixed in the metal fix version of ES1 by disconnecting the DC\_spare \_n routings to the vtrimn pin of TDC at RFE top level ( Figure 19, red and blue connections ) . This solves the issue of the grounded ATB\_N bus , but also makes us lose controllability of vtrimn from external ATB debug pins.

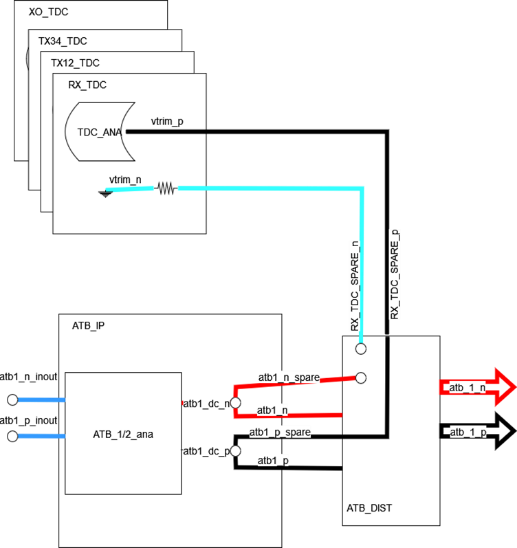


Figure . ATB-TDC connections in ES1-Mfix

## AC ATB Operation

AC ATB interfaces with - RX , RX(WB)-ADC

It is part of characterization test. AC ATB allows monitoring of ac - IF signals from RX from ChirpPLL on external DEBUG\_ATB pins .It also allows forcing of an ac signal from external signal generator to RX-ADC input. AC ATB operation is verified for frequencies up to 40MHz.

AC ATB provides the following connectivity use case options:

<i> external -> internal ( RX-ADC )

<ii> internal ( RX) -> external

<iii> external ( ATB1,2) -> external ( ATB2,1) (loopback)

There is a known limitation due to which it is not possible to observe Vtune ( VCO control signal ) from ChirpPLL via AC-ATB. This will be dealt with in ES2 (**artf905083** ).

### AC ATB connections settings with RFE top

There are 17 differential ac channels on RFE top which connects the AC ATB to RX , RX-ADC and chirpPLL Vtune. The connectivity of these channels is as explained in Table

Table 5. RFE top <-> ACATB channel connectivity table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **AC\_P channel** | | **RFE\_top\_connection** | **AC\_N channel** | | **RFE\_top\_connection** |
| ac\_p | <0> | rx1\_ifbb\_atb\_i0 | ac\_n | <0> | rx1\_ifbb\_atb\_i180 |
| ac\_p | <1> | rx1\_ifbb\_atb\_q0 | ac\_n | <1> | rx1\_ifbb\_atb\_q180 |
| ac\_p | <2> | rx2\_ifbb\_atb\_i0 | ac\_n | <2> | rx2\_ifbb\_atb\_i180 |
| ac\_p | <3> | rx2\_ifbb\_atb\_q0 | ac\_n | <3> | rx2\_ifbb\_atb\_q180 |
| ac\_p | <4> | rx3\_ifbb\_atb\_i0 | ac\_n | <4> | rx3\_ifbb\_atb\_i180 |
| ac\_p | <5> | rx3\_ifbb\_atb\_q0 | ac\_n | <5> | rx3\_ifbb\_atb\_q180 |
| ac\_p | <6> | rx4\_ifbb\_atb\_i0 | ac\_n | <6> | rx4\_ifbb\_atb\_i180 |
| ac\_p | <7> | rx4\_ifbb\_atb\_q0 | ac\_n | <7> | rx4\_ifbb\_atb\_q180 |
| ac\_p | <8> | atb\_adc1\_i0 | ac\_n | <8> | atb\_adc1\_i180 |
| ac\_p | <9> | atb\_adc1\_q0 | ac\_n | <9> | atb\_adc1\_q180 |
| ac\_p | <10> | atb\_adc2\_i0 | ac\_n | <10> | atb\_adc2\_i180 |
| ac\_p | <11> | atb\_adc2\_q0 | ac\_n | <11> | atb\_adc2\_q180 |
| ac\_p | <12> | atb\_adc3\_i0 | ac\_n | <12> | atb\_adc3\_i180 |
| ac\_p | <13> | atb\_adc3\_q0 | ac\_n | <13> | atb\_adc3\_q180 |
| ac\_p | <14> | atb\_adc4\_i0 | ac\_n | <14> | atb\_adc4\_i180 |
| ac\_p | <15> | atb\_adc4\_q0 | ac\_n | <15> | atb\_adc4\_q180 |
| ac\_p | <16> | atb\_chirp\_vtune\_ac\_0 | ac\_n | <16> | atb\_chirp\_vtune\_ac\_180 |

*ac<16> needs attenuating buffer to accommodate full Vtune range : not present in ES1*

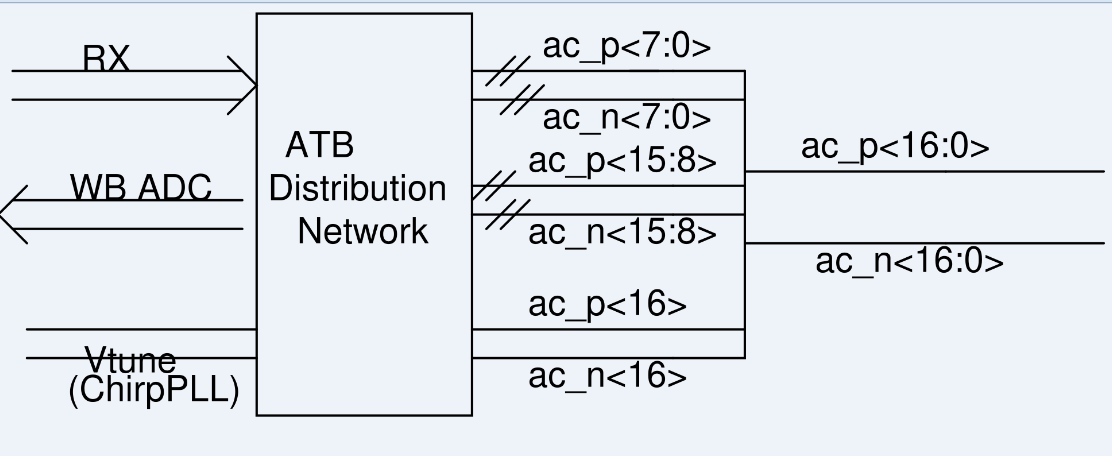


Figure 20.RFE top <-> ACATB channel order

### Internal -> External DEBUG \_ ATB

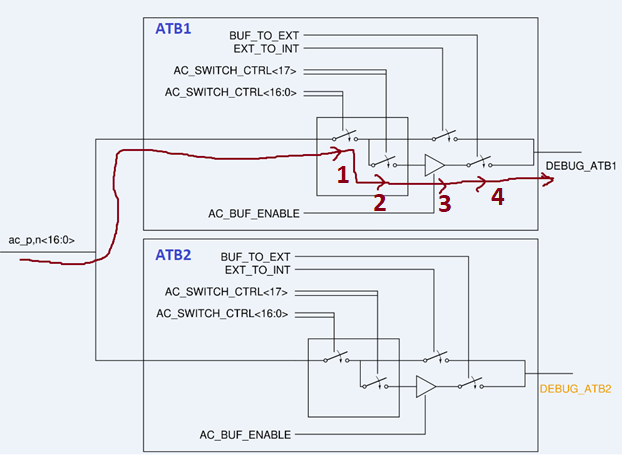
****

Figure 21 AC ATB for internal -> external mode

In order to configure the AC ATB to route an internal ac signal ( say from RX ) to external pins, one has to turn on the path 1->2->3->4 as in figure. Since this use case will most likely make use of the AC buffer, it is implied that only one channel out of the 17 will be active in this mode.

For more details about AC switches and buffer please see [section 4.3.](#_ACATB_Switch)

### External DEBUG\_ATB1 -> internal

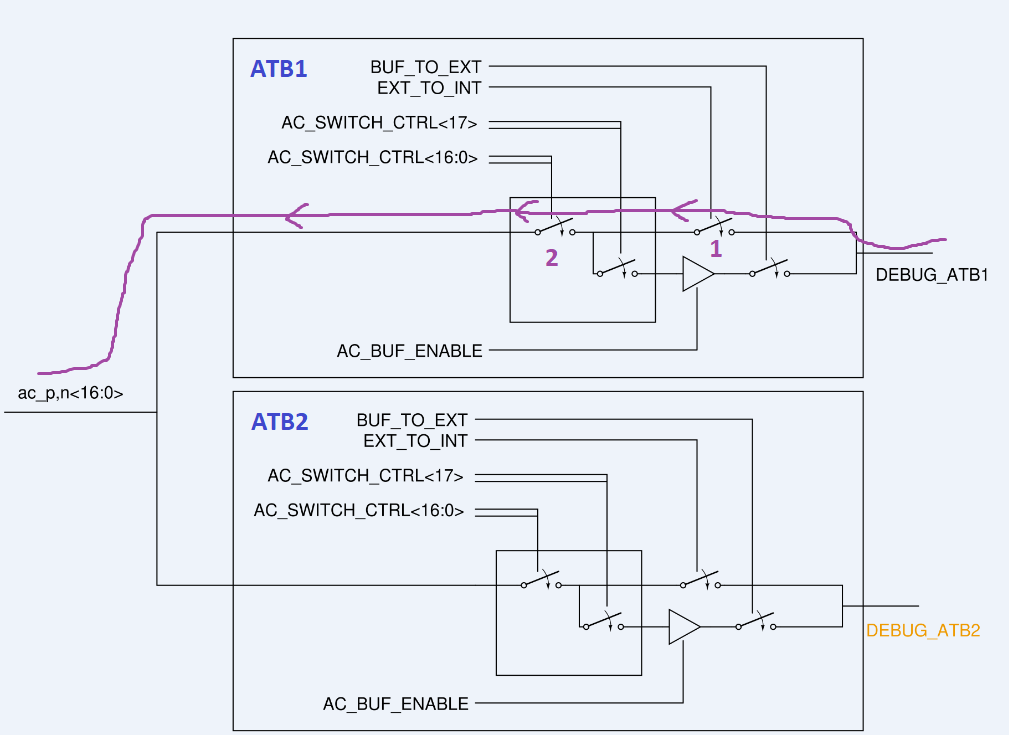


Figure 22. AC ATB for external -> internal mode

In order to configure the AC ATB to route an external ac signal ( say from test signal generator ) to internal node ( RX-ADC input for eg.) , one has to turn on the path 1->2as in figure. Since this use case does not make use of the AC buffer, multiple channels may be active at the same time ( like ADC broadcast mode input )

## Trimming procedure

### Bandgap voltage

The voltage *vref\_0v7* can be trimmed via bits *ctrl\_bg\_set\_dc<3:0>* to target value @125°C (e.g., V=600mV).

The default trim bit settings for the BandGap circuit are described in the Register Map.

Inside ATB, the bandgap is used to provide the reference to BIST ADC. It is not strictly required to trim the bandgap if the ADC is planned to be calibrated for gain ( any error in BG voltage ultimately shows up as gain error in ADC transfer characteristics). Decision pending based on learnings form previous products ( Dolphin )

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### DC ATB Resistors ( Res0 Res1) trimming

[RFE & SOC trim strategy for ES1](https://www.collabnet.nxp.com/sf/go/doc495484)

### ADC Calibration

ATB-ADC gain and offset Calibration is important from FuSa perspective so as to give accurate indications of IP potentials and flag unsafe scenarios.

3 sources of error (uncorrelated) in ADC measurements:

* + BG reference accuracy (gain error)
  + ADC int. LDO (gain error)
  + ADC comparator offset

 The solution to minimizing the error is by doing ADC auto-calibration with *known* voltage.

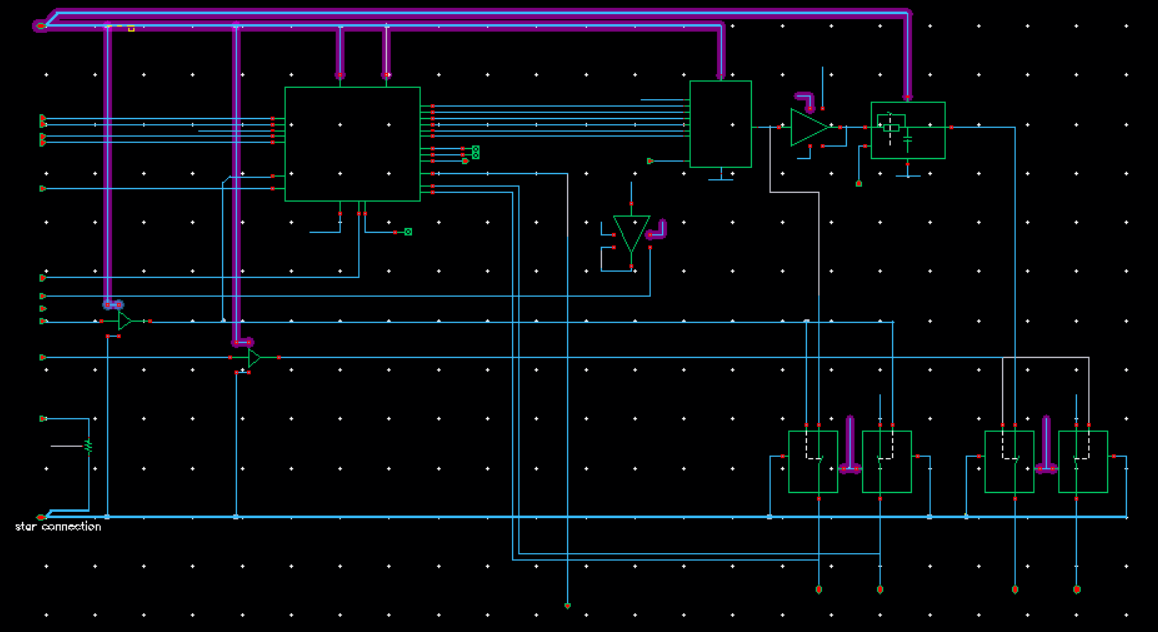
* + The known voltage is coming from the Bandgap 0V9 (AMSIP) @ATB-RFE.

Bandgap offers multiple correlated reference outputs: 0.4 … 0.9V in 100mV steps

and enables 2-point measurement for 1) *gain* and 2) *offset* calibration. Remaining uncertainty is bandgap accuracy

 The ADC calibration procedure is in short :

1. Measure via ADC the Vbandgap value *x* [V]
2. MUX needs to be set to the *x* [V] tap point of the Bandgap
3. Trim (bits *set\_dc[3:0]*) the bandgap output voltage to the expected value *x* [V]
4. Set MUX to the *y* [V] tap point of the Bandgap
5. Measure via ADC the Vbandgap value *y* [V]
6. The difference of the 2 values will provide information on *gain+offset* error



BG taps

Figure 23. ATB- Bandgap taps for ATB ADC calibration

* *x* and *y* are 2 different voltages of the bandgap.
  1. For example:
     + At step 1) one propagates voltage *x* (via MUX) to ADC1
     + At step 3) one propagates voltage *y* (via MUX) to ADC1
     + To select between *x* and *y* one needs to set the MUX correct

# Characteristics

## Static characteristics

Table 7. Static characteristics

TVJ=[-40...+150]°C. Unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the module.

| Symbol | Parameter | | Conditions | | | Min. | | Typ. | | Max. | | Unit |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Tjunction | Junction temperature | | Temperature range in which the IP is within specification | | | -40 | | 50 | | 150 | | °C |
| **Supplies** | | | | | | | | | | | | |
| Vvdda\_1v8 | supply voltage analog domain (Functional Safety) | | functional | | | 1.67 | | 1.8 | | 1.93 | | V |
| operating | | | 1.71 | | 1.8 | | 1.89 | | V |
| Vvdda\_1v45 | supply voltage analog domain | | functional | | | 1.35 | | 1.45 | | 1.55 | | V |
| operating | | | 1.38 | | 1.45 | | 1.52 | | V |
| Vvddd | supply voltage digital domain | | functional | | | 0.84 | | 0.9 | | 0.96 | | V |
| operating | | | 0.85 | | 0.9 | | 0.95 | | V |
| **Power (operating)** | | | | | | | | | | | | |
| IQ,vdda\_1v8 | Quiescent current vdda\_1v8 | |  | | |  | |  | | 100 | | nA |
| IQ,vdda\_1v45 | Quiescent current vdda\_1v45 | |  | | |  | |  | | 100 | | nA |
| I ON,vdda\_1v8 | ON current vdda\_1v8 | |  | | |  | |  | | 15 | | mA |
| ION,vdda\_1v45 | ON current vdda\_1v45 | |  | | |  | |  | | 40 | | mA |
| **Vstress** |  | |  | | |  | |  | |  | |  |
| VSCOVERAGE | | Voltage Stress coverage | |  |  | |  | | 70 | | % | |
| A | | silicon area | |  |  | |  | | 0.503 | | mm2 | |

Rest of the static characteristics are included as part of submodule specifications. ( section 5.2 to 5.8 )

# Test & Debug Implementation

## Introduction

ATB is the test infrastructure for RFE IPs. Internal to ATB , some voltages of interest are connected to the master ATB via the internal ATB submodule as explained in [section 4.8](#_INTERNAL_ATB)

|  |
| --- |
|  |

## Voltage stress

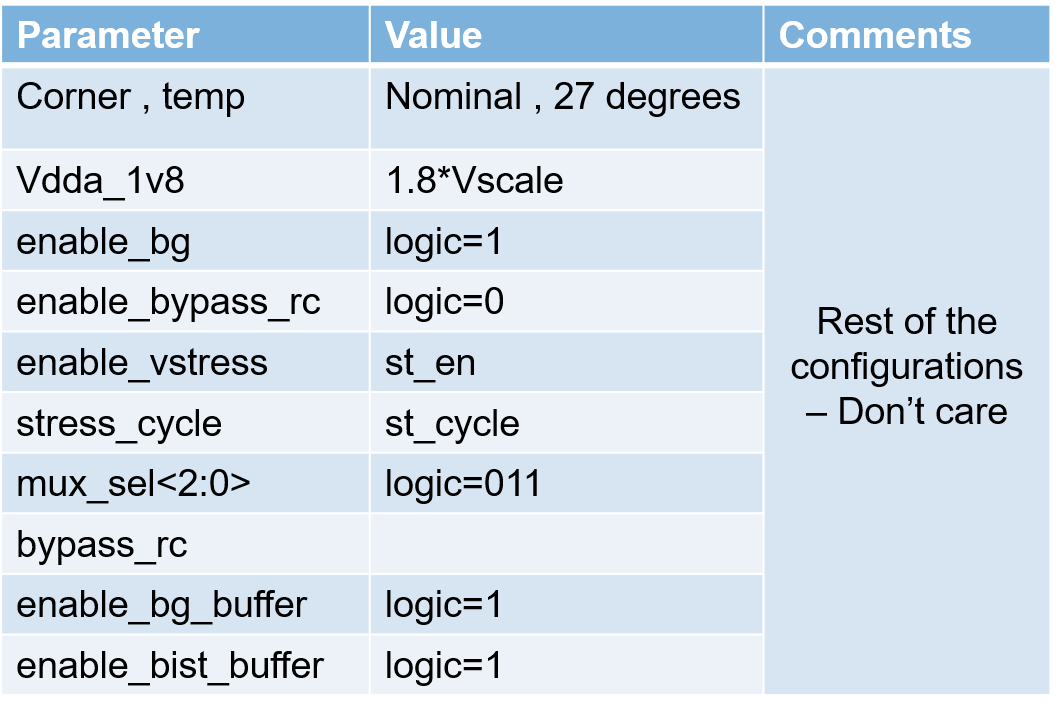
For ATB , the portion which is important from Vstress perspective is the REF BIST and the DC ATB since that is the part which will be active in application/field.

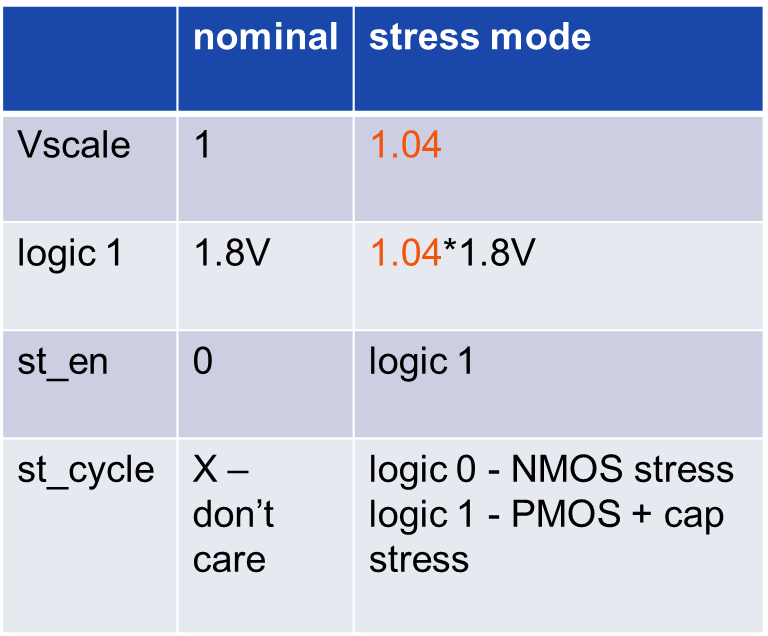
The bit *enable\_vstress* when set to logic ‘1’, puts the module is in voltage stress mode.

For the BandGap circuit, all devices are stressed in two consecutive cycles. When stress\_cycle = '0', NMOS devices are stressed, when stress\_cycle = '1', PMOS devices are stressed.

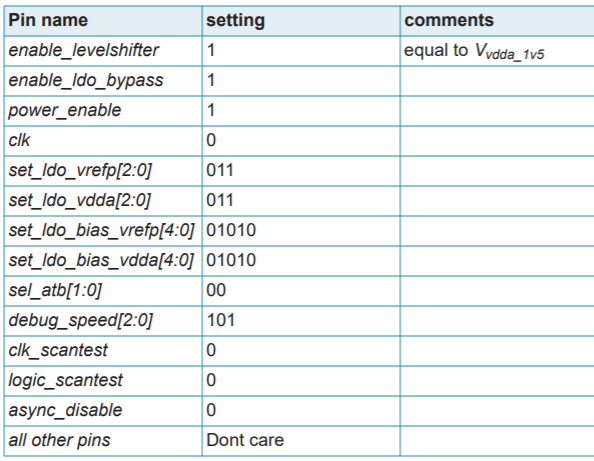
Inside the DC ATB , only the BIST ADC has vstress feature ( by bypassing its internal LDO )

### Settings for putting REF BIST in Vstress mode





### Settings for putting BIST ADC/DC ATB in Vstress mode



### Coverage

Voltage stress mode is implemented at ATB IP and provides a coverage of ~69%. Specification requires coverage ≥80%. To be investigated further and improved in ES2 ( [ATB-RFE does not fulfill the VStress coverage requirement](https://www.collabnet.nxp.com/sf/go/artf906822) )

### limitations

* no Vstress implemented @DCATB switch matrix
* bandgap (BG0V9) cannot be stressed fully as proposed by designer.

#### ES2

Improvement to meet spec of 80%.

# Functional Safety

## DC ATB role in Functional Safety( To be filled – Maxim )

# Process capability - Cpk

To evaluate how the performance of the ATB IP is according to the specification limits, the standard Cpk capability index has been considered:

Cpk= Eq. 4

The Cpk capability index formula takes the assumption of a *normal* (or Gaussian) distribution to predict a certain defect rate. However, not all obtained distributions are normal. In case of *non-normal* distributions, the standard formula cannot be used.

To check the normality of an obtained distribution, a visual assessment of the Q-Q plot and the expanded *Shapiro-Wilk* test (suitable in case of [12-5000] samples) have been performed. Two different options to estimate the capability index in case of non-normality have been considered:

* Data transformation BoxCox
* Quantile-based capability index (Cnpk)

For simplicity of evaluation, the second one has been adopted.

In the evaluation of the Cnpk capability index, instead of using the *mean* (μ) and the *sigma* (σ) parameters as in the Cpk, their equivalent in quantiles in the normal distributions are used.

* mean 🡪 median (X0.5)
* ±3σ contains 99.73% of points 🡪 Quantiles 0.135% / 99.865% to be considered
* Cpk= 🡪 Cnpk=

With the available simulated samples (~250) it is not possible to use the previous quantiles. That is, at least 741 samples are needed. Therefore, quantiles 0.41% / 99.59% have been used which cover 99.18% of points instead of 99.73%.

Cnpk= Eq. 5

Reported results, in case of *non-normal* distributions, will refer to the latter formula.

# Digital design

The digital design document describes the contents of the digital control IP for the ATB IP.

<https://www.collabnet.nxp.com/sf/go/doc497872?nav=1&pagenum=1&pagesize=15>

<https://www.collabnet.nxp.com/sf/go/doc524757?nav=1&pagenum=1&pagesize=15>

# Memory Map

The digital interface is controlled via the so-called *Register Map* and can be found @

<https://www.collabnet.nxp.com/sf/go/doc447863?nav=1&pagenum=1&pagesize=15>

# Physical Implementation

## Technology

Table 8 *Technology information*

| Item | Remark |
| --- | --- |
| Technology (flavor) | TSMC C028HPCP |
| Metal layers used in the IP | 8 |
| DEC | PDK version | DEC 1.54 | PDK 2.5.1 |
| Target DfM level | Recommended rules for analog |
| Supported automotive grade | grade 1 |

## Area

The total area consumed by ATB IP is ≈0.503 mm2.

|  |
| --- |
| **DCATB1**  **DCATB2**  **DCATB1**  **DCATB2**  REF  BIST  RC filter  (REF-BIST)  AC-ATB1  AC-ATB2  ATB  Int  RF-buffer  PPD  LDO  interface  layout *ida\_mmw\_rfe\_atb\_top* |

## Integration details

## Voltage drop

### Shielding

Figure 24. ATB- RFE Layout

# Power Strategy Implementation

# ESD

## On DEBUG\_ATB pins

The DC and AC bus on the external side share the same pins ( DEBUG\_ATB1,2\_p,n). The ESD protection on this pin is as shown in Figure 23.

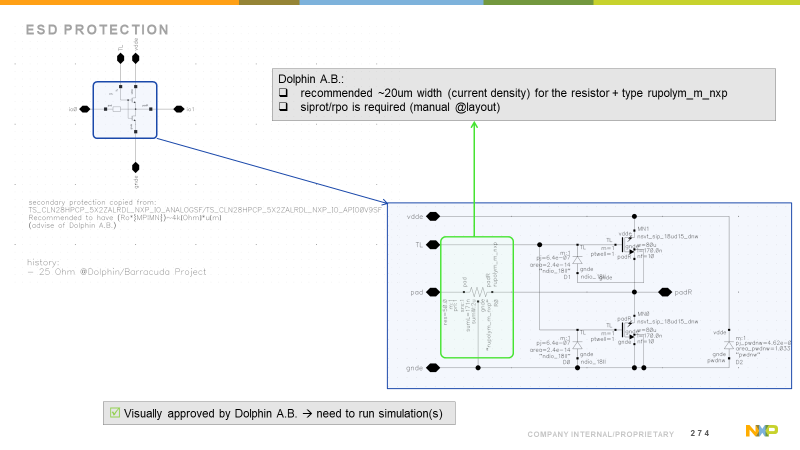


Figure 25. DEBUG\_ATB pins protection

## On PLL\_TEST pin

There is a common ESD protection for PLL\_TEST pin, which protects the interface with both RF buffer and ATB-PPD. The details are as shown in Figure 24 .

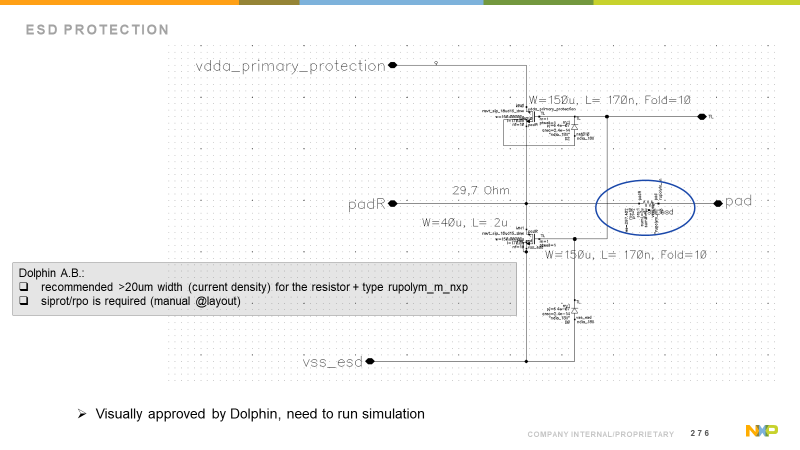


Figure 26. PLL\_TEST pin protection

Apart from this, there are input clamps on RF buffer driver stage.

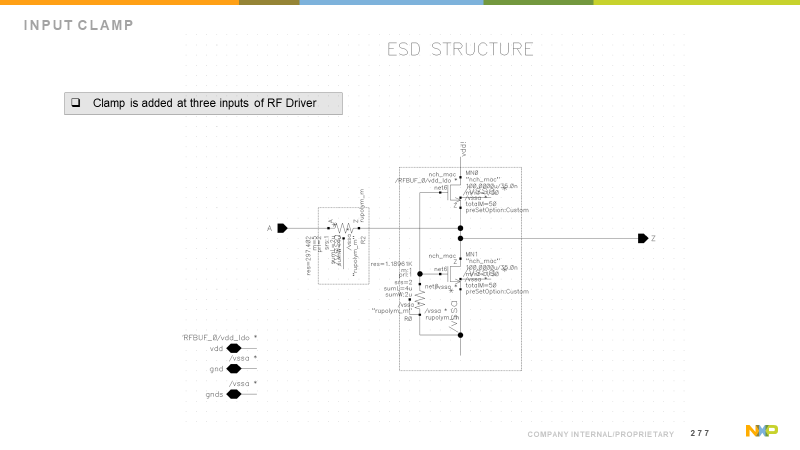


Figure 27. RF Buffer driver stage input clamp

# Interference

# Methodology and Tools

Mainly described in document: <https://www.collabnet.nxp.com/sf/go/doc441840>

|  |
| --- |
| Description of the various methodologies and various tools used which is aligned with DE, T & O team. E.g. refer to the Design rule manuals, Integration tool choices, Reliability Rule checking etc. |

# APPENDIX

# Acceptance Reviews and Approvals

Reviewers

| Name | Role | Location | Date |
| --- | --- | --- | --- |
| Cristian Pavao Moreira | Architect | Toulouse, Fr | <YYYYMMDD> |
| Anton de Graauw | Architect | Eindhoven, NL | <YYYYMMDD> |

Approvers

| Name | Role | Location | Date | Signature  (if required) |
| --- | --- | --- | --- | --- |
| Cristian Pavao Moreira | Architect | Toulouse, Fr | <YYYYMMDD> |  |
| Anton de Graauw | Architect | Eindhoven, NL | <YYYYMMDD> |  |

# Document management

## Abbreviations and terminology

Abbreviations and terminology

| Abbreviation | Description |
| --- | --- |
| RFE | Radar Front End |
| DfT | Design for Test |
| LDO | Low Drop Out |
|  |  |

## Referenced documents

| Doc ID | | Doc Title |
| --- | --- | --- |
| Ref. 1 | | ‘amos\_c028hpcp\_bg0v9\_data\_sheet.pdf’,  <https://nww.sharepoint.nxp.com/teams/13/Analog_Mixed_Signal_IP/Shared%20Documents/Managed%20IP/cmos028hpcp/docs/amos_c028hpcp_bg0v9_data_sheet.pdf> | |
| Ref. 2 | | ‘ATB-Gold Review’,  [https://www.collabnet.nxp.com/sf/go/doc521556](https://www.collabnet.nxp.com/sf/go/doc521556?nav=1&pagenum=1&pagesize=15) | |
| Ref. 3 | | ‘RFE trimming and calibration’,  <https://www.collabnet.nxp.com/sf/go/doc495484> | |
| Ref. 4 | | ‘amos\_c028hpcp\_ad10b5m\_data\_sheet.pdf’,  <https://nww.sharepoint.nxp.com/teams/13/Analog_Mixed_Signal_IP/Shared%20Documents/Managed%20IP/cmos028hpcp/docs/amos_c028hpcp_ad10b5m_data_sheet.pdf> | |
| Ref. 5 | | ‘DCATB switch’  <https://www.collabnet.nxp.com/sf/go/doc532793> | |
| Ref. 6 | | ‘ RFE & SOC Trim strategy for ES1 ‘  <https://www.collabnet.nxp.com/sf/go/doc495484?nav=1&pagenum=1&pagesize=15> | |
| Ref. 7 | | ‘ AMS IP verification report – ATB ‘  <https://www.collabnet.nxp.com/sf/go/doc513571?nav=1&pagenum=1&pagesize=15> | |

1. AI = analog input / DI = digital input / AO = analog output / DO = digital output / AIO = analog in-, output / P = power / G = ground [↑](#footnote-ref-1)